The Ultimate DDR3 Memory Guide

This guide is mostly intended as a reference for the overclocking characteristics of various DDR3 ICs, as well as other potentially useful information. It also covers some basics of DRAM and DRAM overclocking, as well as a short step-by-step guide to getting a simple DDR3 overclock. Note that you are not expected to read through the entire guide, but to read the sections relevant for your goals and the memory you are using. If you are unsure, the Introduction to DRAM overclocking section should get you started.

While this guide is mostly focused on practical overclocking for daily usage, benchmarking usage is also covered for the ICs where it is the most relevant.

It is assumed that you have a basic understanding of memory timings and navigating your BIOS setup. If not, there are many tutorials and articles on the internet which cover this topic. For further reading, I would suggest the JEDEC specification, Micron's documentation, and design guides or scientific articles concerning DDR2, DDR3 and 4.

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Introduction to DRAM overclocking

The basics of DRAM

One of the most important things when it comes to memory overclocking is the ICs or memory chips used on the specific module that you are overclocking. This is what will usually have the greatest impact on what overclocked settings you can run. Third party manufacturers like G.skill and Corsair do not in fact make the DRAM chips themselves, and instead buy them from first party manufacturers like Samsung or Hynix. There are usually significant differences in terms of overclocking characteristics depending on the chip manufacturer, but the same manufacturer can also have different revisions that are vastly different.

DRAM ICs come in different sizes or densities. For DDR3, these are mainly 1 Gbit, 2 Gbit and 4 Gbit, where 1 GB = 8 Gbit. Memory modules typically come with either one or two ranks. One rank is normally a set of 8 memory chips. This means that a single rank module with 2 Gbit chips would have a capacity of 2 GB, while a dual rank 4 Gbit module would have a capacity of 8 GBs. Modules are also often referred to as single or double sided (SS/DS), which denotes the number of PCB sides that are populated with memory ICs. For normal consumer memory, single sided modules are single rank, and double sided modules are dual rank.

An easy way to compare IC density, rank and module capacity is using the following formula:

Module size (GB) = IC density (Gbit) * ranks

It is worth noting that IC revisions are specific to the IC density. For example, 2 Gbit Samsung D-die is completely different from 4 Gbit Samsung D-die, with the former being one of the best DDR3 ICs and the latter being an unimpressive one.

The basics of DRAM overclocking

When overclocking, the main things you will want to adjust are timings and frequency. Both higher frequency and lower timings will have a positive impact on performance. Frequency is often measured as the transfer rate, which is twice that of the actual frequency. Thus, DDR3-1600 will have an actual frequency of 800 MHz, and DDR3-2400 will run at 1200 MHz. The transfer rate will often be referred to as the frequency in MHz (for example, DDR3-1600 being referred to as "1600 MHz"), which is technically incorrect. This guide exclusively uses MHz to refer to the actual memory frequency.

It helps to think of timings in terms of latencies. Here, a specific latency would be the amount of time it takes to complete a specific memory operation. This time is usually constant across large

frequency ranges, assuming the same voltage. Timings are a way to express these latencies in terms of clock cycles. A timing of 12 ticks would mean a latency of 12 clock cycles for that specific operation. Thus, a timing of 6 at 400 MHz would yield the same latency as a timing of 12 at 800 MHz since the clock cycles only take half as long at 800 MHz.

Since many memory operations tend to have the same minimum latency regardless of memory frequency, you will need to step up these timings as you step up the frequency. If the minimum timings you can run at 800 MHz are 8-8-8, you would need to run 12-12-12 at 1200 MHz for similar stability. See the formulas section near the end of the document for useful conversion formulas.

Stability testing and general overclocking methodology

One of the most central parts of memory overclocking is testing the stability of your overclocks.

The following are some popular memory tests:

- HCI MemTest (Windows/bootable)
- MemTest86 (bootable)
- TestMem5 (Windows, needs a good config to be effective)
- Karhu RAM Test (Windows, paid)
- Google stressapptest (Linux, can be used on a portable USB drive distro)
- Prime95 blend/large FFTs with high memory usage (effective for IMC testing)
- OCCT (Windows)

For the tests that run in Windows, I would recommend creating a separate Windows installation for memory testing, as unstable memory has a tendency to corrupt Windows. If this is not an option, I would recommend at least performing some initial testing in a bootable memory test, before moving on to testing in Windows.

The general overclocking and stability testing methodology is to optimize a setting until you no longer get POST, then step it back to the best setting that did POST and test stability. If it is stable, you can move on to the next setting. If it is unstable, you'll want to revert the setting one step further and repeat the process of stability testing and reverting until you reach stability. The reason for "finding stability" instead of "finding instability" is that instability typically appears quickly in memory tests, while you might spend hours testing stable settings until you get to unstable settings if you try to "find instability" instead.

Basic overclocking procedure

The first step to overclocking would be to find the maximum frequency that your memory setup will run. If you have no info on the ICs used, a good place to start would be 1200 MHz with 12-15-15-35 timings, 2T command rate, 16 tFAW (subtiming) and 1.65 V DRAM voltage. If it is unstable or doesn't POST, set 11-14-14-32 timings instead and step down frequency until it is stable.

For a frequency that POSTs but is unstable, you can try playing around with the voltage slightly (though see the section about DRAM voltage tolerance for ICs and memory controllers). Most ICs will either benefit from or remain unaffected by higher voltage, but a few may benefit from lowering the voltage. Going above 1200 MHz is an advanced topic which may result in worse performance if not done correctly; I would thus not recommend it for most users. However, for those interested, it is covered in the advanced section.

Minimizing timings does not need to be done in any particular order, however I suggest starting with the tCAS timing (also known as CAS Latency or CL/tCL). Reduce it to the minimum value that POSTs. If this value is only moderately unstable, you can typically stabilize it by increasing the DRAM voltage. I would recommend going in increments of 20 mV at a time until you reach stability. However, see the section about DRAM voltage for ICs and memory controllers before increasing voltage.

The rest of the primary timings typically do not benefit much from increased voltage; as such, if a certain value is unstable, you will usually need to run the next value above it that is stable. Minimize these one at a time. If you know which ICs you have, you can use the typical timings for that IC, scaled to the frequency that you are running, as a starting point. See the formulas section for info on how to scale timings for frequency.

Now that you have found your maximum stable frequency and minimum stable primary timings, you can start moving on to the secondary timings. Start by trying tRRD 4. This will in most cases be stable, but 5 or even 6 may sometimes be required, especially with 4 Gbit ICs. Refer to your specific IC in the DDR3 ICs section for more information. Next is tRFC. For this one, the gap between no POST and fully stable is typically very small. Step it down in steps of 10 until no POST, then set it 10 ticks higher than the minimum value that did POST. This will nearly always be stable unless the memory heats up a lot during operation. As a starting point, refer to the Identifying IC characteristics table towards the end of the document and start with a value a bit above the typical tRFC for your IC. Note that the values in the table are in nanoseconds, so you will need to convert them to ticks based on your frequency (see the Formulas section). If you do not know your IC, simply start at the auto value for tRFC.

For tRTP, set 3 (or the minimum configurable if higher), and for tWTR, set 4 on Haswell and later Intel or 6 on everything else. These values should always be stable. The performance

impact from these two timings is relatively minor so there is not much point to minimizing them fully. The tWR and tREFI timings have a tendency to produce very intermittent errors and tuning them is thus more of an advanced topic (covered in the next section for those interested). Their performance impact is not that great either. Finally, you can try 1T command rate. Commonly, if it POSTs, it is stable.

Finally, when you've found your minimum stable timings, you can optionally minimize the DRAM voltage. You can start by reducing the voltage by 50 mV at a time until you reach instability. Then increase the voltage in 10 or 20 mV steps until you are stable again. I typically increase the voltage a further 10–20 mV beyond the minimum stable for some extra margin. If you plan on optimizing the remaining sub-timings, I would recommend doing this step after that process is complete.

Advanced tuning

Above 1200 MHz

For running above 1200 MHz, one important aspect to consider is the tCCD timing. This timing directly controls how close together reads and writes can be performed. Thus, if frequency is increased but tCCD is increased more than the frequency, this will result in worse performance for nearly all situations. By default, motherboards start setting tCCD higher than the minimum value of 4 at 1300 MHz and above. Certain MSI motherboards may even start doing this at 1200 MHz. Many ICs also start requiring increased tCCD when pushing above 1200 MHz.

On Intel (and presumably also AMD), the tCCD timing is split up into two timings. For Haswell, this is tRDRD for the minimum delay between reads and tWRWR for writes. On Sandy/Ivy Bridge, I believe tRRSR corresponds to tRDRD and tWWSR to tWRWR. For even older platforms, you are unlikely to be running >1200 MHz to begin with for daily, so this is not a concern.

As a quick rule of thumb, you want to be able to run at least 20% higher frequency for tCCD 5 to be worth it compared to tCCD 4, though this can vary depending on the application. If tCCD > 4 is only required for either reads (i.e. tRDRD) or writes (tWRWR), the frequency increase required for it to make sense tends to be smaller. For example, 1400 MHz tRDRD 5 tWRWR 4 is often beneficial compared to 1200 MHz tRDRD/tWRWR 4. If it is only tWRWR that needs to be higher than 4, the frequency gain required is even less, since read performance is typically more important than write performance. I recommend finding the maximum frequency with both tCCD 4 and 5 to see how big the difference is. If the difference is only minor (eg. 100 MHz or less), it is usually better to run tCCD 4.

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Another concern when pushing higher frequency is maximum supported CL. High frequencies may require high timings in tick values. However, some ICs do not support high CLs and will not POST if they are set. Maximum supported CL can be tested at a low frequency such as 800 MHz. If it POSTs, the IC supports that CL, and there is no need to test further. For finding maximum frequency beyond 1200 MHz, set the maximum supported CL that you found at lower frequency, tRCD/tRP 18 and tRAS 40. Step up frequency until unstable.

When you have found your maximum stable frequency and if applicable, decided on which frequency/tCCD compromise makes most sense, start minimizing timings as described in the previous section.

tREFI and tWR

The tREFI timing is a bit special since it configures how often your memory should refresh. During refreshes, the DRAM is unable to complete other operations, and thus a higher tREFI (meaning less frequent refreshing) equates to better performance. tREFI is extremely sensitive to temperature; a 10 °C increase usually results in half the tREFI being required. As such, it's hard to give recommendations since just a few degrees Celcius different temperature will require vastly different tREFI. I suggest stress testing them thoroughly at a worst-case temperature that your system might reach. Keep in mind that a GPU in a poorly ventilated case might heat up the RAM to a higher temperature than you would reach during a standard memory test. To achieve higher internal case case temperatures, you may lower case fan speeds or unplug them entirely. The CPU cooler fan is best left alone. Note that Sandy and Ivy Bridge CPUs appear to universally have some odd behavior where setting tREFI too high will cause the system to not POST, even if the DRAM can handle it. The maximum value tends to be somewhere in the 10k range, and it is usually stable unless the DRAM gets very hot.

For tWR, 5 is almost always stable on Hynix and Samsung ICs. On Nanya and Micron ICs, it can vary greatly from sample to sample, even within sticks from the same kit. Some will be able to run 5 while others may require more than twice that. Elpida and PSC ICs are more consistent. These will often need a bit more than 5 at higher frequency, commonly 6–10, though the 2 and 4 Gbit Elpida/PSC ICs that don't clock above 1000 MHz may for some samples be fine with 5.

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Module manufacturers

G.Skill

The first 4 digits of the G.Skill serial number are the date code. 1241 would be week 41 of 2012, in other words. The 6th digit indicates IC manufacturer. For modules from early 2012 and before, 2 is Hynix, 3 is Samsung, 6 is Elpida and 0 is PSC. After early 2012, the manufacturer codes changed, with 5 for Samsung, 4 for Hynix, 1 for Nanya, 8 for Elpida and 3 for Micron. The 5th digit might be related to the JEDEC bin, as 1 typically seems to be PC3-10600 rated ICs and 2 typically PC3-12800. G.Skill modules from after mid 2017 use the same IC code as DDR4; see my DDR4 guide for more info.

The number of ranks on the module can be determined simply by observing if there are chips on both or only one of the PCB sides, when looking between the heat spreaders. This information, in combination with the IC manufacturer, date code, module size and XMP bin, should be able to give you an idea of what ICs to expect on a module. Refer to the XMP guide for more info.

One thing to note about G.skill is that they tend to bin their modules very hard for specs beyond basic 1600 9-9-9 and similar. I've come across modules that have as little as a 20 mV voltage margin on the XMP and start causing errors in memory tests in a poorly cooled environment. This usually means that you won't have much headroom for overclocking, at least not in terms of timings. You can however often overclock them quite a bit in terms of frequency, given that you scale the timings up linearly, and that the ICs on the specific module can handle it.

Corsair

Corsair has a really easy way to identify the ICs used on their modules. Simply look for the version number ("ver x.xx") on the sticker and compare it to the table below.

Version	IC	Note
2.1	Elpida 1 Gbit	Usually BASE (Hyper)
2.2	Elpida 1 Gbit	Usually BBSE/BBBG
2.3-2.5	Elpida 1 Gbit BDxx/BFxx	
2.12	Elpida 2 Gbit BCSE/BDBG	
2.13	Elpida 2 Gbit BDSE/BDBG	Rare

2.2x	Elpida 4 Gbit	
3.1	Micron V48A/V58B	V48A on 2007-2008 date code, V58B on later
3.2	Micron V48C	2011+ date codes may contain other ICs
3.5	Micron V58B	
3.7	Micron V68A	Suspected based on characteristics, rare
3.9	Micron V88A	Suspected, extremely rare
3.13	Micron V69A	Rare
3.17	Micron V79B	Very rare
3.19	Micron V79D	Has also been seen on an 8 GB module, somehow
3.23	Micron V70S	Rare
3.24	Micron V80A	D9QBJ or SpecTek PEB12
3.28	Micron V80B	Rare, suspected based on characteristics
3.29	Micron V80B & V99B	Suspected based on characteristics
4.1	Samsung 1 Gbit D-die	
4.13	Samsung 2 Gbit D-die	
4.19	Samsung 2 Gbit various	P/Q/T- and likely S-die, somewhat rare
4.21	Samsung 4 Gbit B-die	
4.23	Samsung 4 Gbit D-die	
4.29	Samsung 4 Gbit Q-die	
5.x	Hynix 1 Gbit	
5.11	Hynix 2 Gbit BFR	
5.12	Hynix 2 Gbit CFR	
5.13	Hynix 2 Gbit DFR	Very rare
5.14	Hynix 2 Gbit EFR	Rare
5.20	Hynix 4 Gbit AFR	

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5.21	Hynix 4 Gbit BFR	
5.23	Hynix 4 Gbit DFR	Rare
5.29	Hynix 4 Gbit MFR	
7.1	1 Gbit PSC 1st gen.	
7.5+	1 Gbit PSC 2nd gen.	
7.1x	Usually 2 Gbit PSC	1 Gbit second gen. PSC has occurred in 7.13. Rare
7.2x	4 Gbit PSC	Rare
8.x	Nanya 1 Gbit	
8.11	Nanya 2 Gbit B-die	Rare
8.14	Nanya 2 Gbit E-die	Extremely rare
8.15	Nanya 2 Gbit F-die	Rare
8.16	Nanya 2 Gbit G-die	
8.19	Nanya 2 Gbit I-die	Very rare
8.21	Nanya 4 Gbit B-die	Very rare
8.22	Nanya 4 Gbit C-die	
8.23	Nanya 4 Gbit D-die	Somewhat rare

In general, avoid Corsair's black Vengeance DDR3-1600 9-9-9 4 GB modules. A large portion of them (likely more than 50%) are based on Elpida 2 Gbit BCSE, which is practically un-overclockable, while the second most common IC for them is Nanya G-die, which is worse for overclocking than most 2 Gbit ICs. Their DDR3-2133+ kits and kits with tighter timings at lower frequencies (such as DDR3-1600 8-8-8 or lower) are generally quite good. Some of their XMS3 modules and most of their colored Vengeance 4 GB modules seem to use Hynix 2 Gbit chips, which are a fair option for overclocking. 8 GB modules and 4 GB modules from 2014+ use all kinds of various 4 Gbit ICs, which typically overclock quite well in terms of frequency.

Corsair generally does not bin as strictly as G.skill, meaning that you usually get more overclocking headroom. Some of their higher end 8 GB modules are great for this reason. I’ve personally had great success with many of their Dominator modules rated at tight timings for the given frequency.

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Kingston/HyperX

Kingston seems to mostly use Hynix, Micron and Elpida chips for their modules. I would stay away from their OEM/OEM-style modules without heat spreaders, since they usually either use poor Elpida ICs, or have poor PCBs that ruin the overclocking potential of otherwise good ICs.

Most of their HyperX kits use Hynix and Micron ICs which overclock quite well. Though, if you're looking for top DDR3, they may not be the best option, since Micron ICs that aren't on Crucial kits usually aren't especially good, and Hynix ICs don't do particularly low timings, even if they overclock well in terms of frequency.

Kingston non-OEM modules come with an 11 character code that is typically vertical on the specs sticker, for example APMH1661329. This code tells you the IC manufacturer, year and number of ICs on the module.

4th letter: First letter of the IC manufacturer (H – Hynix, M – Micron, E – Elpida, K – Kingston rebrand)

5th and 6th digit: Number of ICs (8 for single sided, 16 for double sided and 18 for double sided ECC)

8th and 9th digit: Manufacturing year (13 for 2013, for example)

Crucial

The Crucial brand is owned by Micron, and thus almost exclusively uses Micron ICs. Crucial modules from the higher-end line ups, such as Ballistix Tactical, Tracer or Elite appear to use modified versions of the standard Micron ICs which can do way lower timings, and are often some of the lowest-timing modules available in 4 and 8 GB capacities. Note that these modified versions are not known to appear on more basic models, such as Ballistix Sports or modules without heat spreaders.

At the end of the Crucial part number on the module sticker, there is a code starting with a period, usually followed by an M. The next number (either 8 or 16 for non-ECC modules) indicates the IC count. 8 is thus a single rank and 16 are dual ranks. This means that the IC density (in Gb) is the same as the module capacity (in GB) for 8, or half for 16. Usually, an F follows the number. The letter after the F (if present) indicates the die revision as per Micron die revisions (not design IDs). If there is a 2 at the end of the part number, this indicates that the IC was originally double the active capacity, with half of it disabled. For example, a .16FER2 code on a 4 GB module indicates 4 Gbit E-die which has been down-binned to 2 Gbit density.

OEM modules

OEM modules are those made directly by the first party manufacturers, usually for use in OEM systems like those from Dell and HP. OEM modules can be a great way of getting reasonable modules for very cheap, since most buyers are scared by their lack of heat spreaders. One of the biggest advantages of OEM modules is that you can be certain of which ICs they use based on just their model number. This allows you to buy modules based on known-strong ICs.

For 4 GB modules, I would recommend Samsung ones based on C- or D-die, or single rank Hynix ones based on AFR and BFR (preferably 15xx date code for BFR). Modules based on 4 Gbit Samsung Q-die are also reasonable.

For 8 GB modules, I can only recommend Hynix ones based on AFR and modules based on Samsung Q-die, as others typically won't run 1200 MHz with reasonable timings. On Sandy Bridge where the memory controller is limited to 1066 MHz, OEM modules based on MFR and 4 Gbit Samsung B-die are also a good option.

I would recommend avoiding Micron, Elpida, Nanya and Kingston OEM-style modules, as they are usually either using poorly performing ICs, or are let down by bad PCBs that limit their overclocking potential.

DDR3 ICs

It can be assumed that results apply for voltages around 1.65 V if no other mention is made. Results are for memory test stability with active fan cooling on the memory unless stated otherwise.

Hynix

1 Gbit AFP

Found on various low and standard bin third party modules from the early DDR3 era, and even some from early 2010. Possibly the worst mass production 1 Gbit IC, only beating bad samples of Elpida BASE/BABG, but getting beaten by good samples. Maximum frequency is between 900 and 1100 MHz, though 1100 MHz is rare. Expect timings like 11-11-10 at 1000 MHz or 10-10-9 at 933 MHz. Voltage scaling is dubious; there is no apparent scaling above the standard voltage range, though certain timings may encounter voltage limits if trying to run low voltages.

1 Gbit BFR and TFR

These are similar in characteristics and therefore grouped together. In fact, there seems to be some confusion within Hynix about which one is actually the second generation 1 Gbit IC, with both being referred to as second gen in different places. Both are based on the same manufacturing process (54 nm) as well. They seem most common on Hynix OEM modules from 2009 and 2010, but BFR also appears on low and standard bin third party modules every now and then.

For BFR, maximum CL is 11 (with maximum CWL 8, which is usually auto at CL 11). It is possible that this is a limiting factor for frequency, as all tested samples have needed CL 11 at their maximum attainable frequency. Neither tCAS nor frequency at the CL 11 maximum scales reliably above 1.7-1.8 V. Maximum frequency is commonly 1100 with some samples hitting 1200 MHz. TFR seems to hit similar maximum frequencies and is not limited by maximum CL for frequency as it is able to run up to CL 13 and CWL 9.

For TFR, expect 10-12-10 or 9-12-10 timings at 1100 MHz depending on voltage, with some samples needing tRCD 13. For BFR, 11-12-11 at 1200 MHz or 11-11-10 at 1100 MHz would be typical. tRAS runs low as is typical with Hynix. No timings other than tCAS scale notably with voltage.

1 Gbit DFR

Only seen on Hynix OEM modules from late 2010 onwards. One of the better 1 Gbit ICs for frequency, typically reaching around 1333 MHz with standard voltages. Higher is also possible if pushing really high voltages.

Typical timings at 1200 MHz would be 10-12-11-12 at around 1.7 V. tCAS scales well with voltage. tRCD only scales slightly, at approximately 1 ns/V in the standard voltage range, with greater scaling at lower voltages and worse scaling at higher voltages, up to over 2 V. tRP does not seem to scale above ~1.6 V.

tRFC is approximately 70 ns, only scaling a few ticks over the entire voltage range. tRRD should run 4 even at higher frequencies. tRDRD 4 was also tested to be stable at 1400 MHz, which is better than most ICs which require 5, severely limiting the maximum bandwidth at high frequencies. CWL scales well with voltage and runs rather low.

2 Gbit AFR

2 Gbit AFR is quite rare. I've only found it on 4 GB Kingston and Hynix OEM modules from 2009 and early 2010. Later 2010 modules tend to be based on BFR.

They're not especially good for overclocking, but also not horrible. Will do between 1066 and 1200 MHz depending on the module quality. Typical timings at around 1.65 V would be 11-13-11 for 1200 MHz and 10-12-10 for 1100 MHz. Seems to be less temperature sensitive than BFR.

2 Gbit BFR

2 Gbit BFR is typically found on high performance 2 Gbit-based modules from 2010 and 2011 as well as standard performance 2 Gbit modules from 2010–2012. Nearly all early high performance 4 GB modules such as DDR3-1600 7-8-7 or higher frequencies will be based on BFR. 2 Gbit BZR also exists, which can be considered equivalent.

Dual rank modules will typically be able to run maximum frequencies of around 1200 MHz. The max frequency range is generally between 1150 and 1250 MHz at 1.65 V depending on the module. Single rank modules may run higher frequencies, with up to 1466 MHz being tested successfully.

tCAS scales well with voltage. The relation is often ideally linear or close to it. tRCD does not scale at all with voltage. tRP scales very slightly at roughly 0.8 ns/V between 1.50 and 1.65 V, with very minimal scaling above 1.70 V. Exact timings vary a lot depending on module quality. Poor ones will run 11-13-11 at 1200 MHz, while the best ones will do 9-11-9 in the 1.6 V range. Modules with better tCAS performance tend to also have better tRCD and tRP performance.

Note that 2 Gbit BFR is quite temperature sensitive. Overclocking performance might be significantly worse if "cooled" by the hot exhaust air from a high power graphics card, compared to actively cooled by ambient temperature air, or with airflow around the memory. A fan with a reasonable RPM pointed at the RAM is highly advantageous when running above 1.65 V.

2 Gbit CFR

Typically found on 4 GB DR and 2 GB SR Hynix OEM modules from 2011 and 2012. Also present on many high speed (DDR3-2133+) third party 4 GB modules from 2012. Most DDR3-2600/2666 CL11 and all 2800 modules from 2012 should be based on CFR.

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The IC is one of the harder 2/4 Gbit ICs for Intel IMCs. Single rank modules can run high speeds with no problems. Double sided modules (both third party and OEM) tend to hit IMC limits around 1400 MHz on Haswell. Certain samples also appear to have the ICs themselves struggle at around this speed, though this may be related to PCBs. Typical timings at 1200 MHz would be 10-12-11 at 1.60–1.75 V for unbinned modules. High bin modules will be slightly better.

tCAS scales well with voltage, though the relation is not quite ideal. tRP scales somewhat with voltage, though not nearly as well as tCAS. tRCD voltage scaling is very minimal. A certain voltage might be required for a tRCD latency that is right at the limit, but increasing voltage will not allow lowering it significantly below that.

CFR is somewhat unique among 2 Gbit ICs in that it requires tRRD 5 at 1200 MHz, compared to 4 for most others. tRFC is quite low for 2 Gbit ICs, with an expected range of 85–100 at 1200 MHz. CWL 5 should not be an issue assuming typical or high voltage.

2 Gbit DFR

Seems to be quite rare. Found on third party modules ranging from standard DDR3-1600 to higher end DDR3-2400.

Maximum frequency will be somewhere around 1200 MHz. Some samples will be limited to 1100 MHz without pushing extra voltage, while others will reach 1300 MHz. Typical timings at 1200 MHz would be 10-12-12-12 at around 1.65 V.

tCAS scales ideally with voltage up to the 1.8 V range. There is scaling well beyond 2 V, though it is significantly worse than at lower voltages. tRCD scales at more than 6 ns/V at less than 1.4 V, dropping to 2 ns/V for the 1.6 and 1.7 V range, finally hitting a scaling limit a bit above 2 V. tRP only scales slightly up to around 1.5–1.6 V before it rolls over and starts scaling negatively.

Expect a bit under 100 ns tRFC. tRFC takes a fairly large hit when going below 1.5 V, but does not scale significantly above that and even rolls over slightly at high voltages. Should run CWL 5 unless at low voltages.

2 Gbit EFR

Main IC used on 2 Gbit-based Hynix OEM modules from late 2013 onwards. Seems to be rather prevalent on late DDR3 era 2 GB modules from third party manufacturers, but only rarely appears on 4 GB modules.

There are two categories of this IC which have distinct frequency behavior. The first is OEM modules from around 2014. With tCCD 4 (auto at and below 1200 MHz), they tend to max out

around 1000 MHz. Setting tRDRD to 5 increases the clock limit to around 1200 MHz, which is likely a worthwhile trade for performance. The second category is (Corsair but potentially other) third party modules from the later DDR3 era. On these, frequency scales well with voltage unlike the ~2014 OEM modules, and they commonly reach around 1400 MHz if pushing voltage into the 1.7 V range. There appears to be little or no frequency scaling above 1.8 V.

Typical timings at 1000 MHz would be 9-10-10 at around 1.5 V, or 11-12-11 at 1200 MHz. tCAS scales well with voltage up to around 1.8 V. tRP scales somewhat with voltage, typically requiring a 400 mV voltage increase going from 10 to 9 at 1000 MHz.

2 Gbit FFR

Nearly impossible to find. The best chances are probably on 2 and maybe 4 GB modules of basic bins from the later DDR3 era, around 2016. Note: results based on only two tested samples from the same batch.

Frequency is very impressive, easily hitting 1500 MHz at low voltages (~1.4 V). Higher could not be tested due to motherboard issues, but scaling up until that point suggested it would likely reach 1600–1700 MHz and possibly higher. Of note is that tRDRD 4 and tWRWR 4 were stable at 1500+ MHz, which is the only IC I've tested so far that can handle such high tRDRD 4 frequencies.

tCAS is very strong, similar to 2 Gbit Samsung D-die. One unbinned sample ran 1200 MHz CL 9 at 1.70 V and 1400 MHz CL 9 at a bit over 2.2 V, which is similar to above-average D-die. Scaling is good, being roughly ideal up to around 1.75 V and successively dropping off slightly at higher voltages. tRCD and tRP ran at around 9.3 ns depending on the voltage for both tested samples. For reference, this would be 13 ticks at 1400 MHz and 11–12 at 1200 MHz. tRCD scales notably at roughly 2 ns/V between 1.5 and 1.6 V. The scaling is greater at lower voltages, approaching ideal at below 1.3 V, and progressively worse at higher voltages, with tRCD plateauing somewhere around 2 V. tRP on the other hand scales negatively above 1.4 V. The degree of this negative scaling varied between the two samples, with one losing 0.3 ns from 1.4 V to 1.9–2.4 V and the other one losing 0.9 ns from 1.4 V to 2.2 V. In general, expect tRCD and tRP to run similar values at around 1.5 V, while tRP may need to be one tick higher than tRCD at high voltages.

tRRD scales with voltage up to around 2.1 V. tRRD 4 required 1.35 V at 1066 MHz, 1.5 V at 1200 MHz and 1.8 V at 1333 MHz, before finally maxing out a bit below 1400 MHz at the scaling limit of ~2.1 V (tested in 50 mV increments). tRFC scales positively by a few ticks at

below 1.65 V, and negatively by a few ticks above 1.8 V. Expect around 90 ns, or 108 ticks at 1200 MHz.

2 Gbit GFR

Similar to FFR in rarity and where one might expect to find it, though with the optimal time frame likely being 2017 and newer. Note: results based on only two tested samples from the same batch.

Frequency is quite good, hitting 1400 MHz with ease and doing 1466 MHz and above with higher voltages. Timings are reminiscent of 2 Gbit D-die, doing 1200 MHz 9-11-11-11 at 1.74 V for the better module. With some binning (which is practically impossible due to the rarity of these), it would likely be possible to achieve timings similar to good bin D-die, like 1400 MHz 9-12-12.

Maximum voltage regardless of timings and frequency was 2.28 V on one of the modules. tCAS scales well, but not quite ideally. tRCD only scales up to around 1.65 V. While it does get as high as 5 ns/V at below 1.2 V, scaling at any voltages which are likely to be used is minimal. tRP scales better, starting at over 3 ns/V below 1.3 V, dropping to ~1 ns/V at around 1.65 V and continuing to scale to over 2.1 V, though not to any significant extent.

tRFC is not especially impressive at around 100 ns. A significant voltage increase might allow a few ticks lower tRFC. tRRD also scales with voltage. At 1.65 V and above, 4-16 was possible at 1200 MHz, though even at high voltages 5-20 was required for 1400+ MHz. Unlike most Hynix ICs, CWL could not be minimized to 5. CWL also gets worse at less than 1.65 V. One noteworthy timing characteristic is the ability to run tRDRD 4 at 1400 MHz, compared to 2 Gbit D-die which usually requires 5, resulting in a significant loss in maximum bandwidth.

4 Gbit MFR

Typically found on high frequency third party modules. Nearly all 1300+ MHz and all 1400+ MHz 8 GB modules are based on MFR. Common on 2013 DDR3-2400 modules from Kingston, though these are often also 4 Gbit AFR. Sometimes used on lower speed modules such as 1600 and rarely 1333. Rather common on ADATA's 1600 modules from the right time period. Also found on OEM modules with the corresponding part number.

The variation on these modules is quite large. I will divide them into three rough categories based on strength: *Good*, *Typical* and *Trash*. *Good* modules that do settings typically associated

with MFR are almost exclusively found on DDR3-2800+ bins (potentially 2666 CL 11 as well, though seemingly not CL 12). Modules from 2133 and 2400 bins largely all fit into the *Typical* category. Many OEM modules and some 1600 bin modules also make it into this category, while the remaining fit into the *Trash* category.

For frequency, there are two main frequency limits to consider: tCCD-limited frequency and fundamental frequency. tCCD-limited frequency is when higher tCCD (eg. tRDRD and tWRWR) would allow higher clocks. For this, it is usually tRDRD that is the limit first rather than tWRWR. While tRDRD does scale slightly with voltage, the scaling isn't enough to increase the max tRDRD 4 frequency by much more than 100 MHz. On the other hand, tWRWR scales more significantly with voltage, meaning it is usually possible to run it at 4 at frequencies requiring tRDRD 5, given enough voltage.

On *Trash* modules, the tCCD 4 limit may be as low as 1100 MHz at 1.65 V, with 1200 MHz requiring above 1.7 V if possible (limited by tRDRD). For *Typical* modules, 1200 MHz tCCD 4 usually has voltage requirements in the 1.4 V range and 1300+ MHz tCCD 4 is often possible. *Good* modules vary quite a bit for tCCD-limited frequency, likely since this isn't what they're binned for, with some having similar tCCD 4 frequency limits and voltage requirements as *Typical* modules, while others are significantly stronger.

For frequency not limited by tCCD (eg. tCCD 6, typical auto value at 1400+ MHz), the results vary significantly; some *Trash* modules need close to 1.8 V for just 1300 MHz and don't scale further with voltage, while top bin MFR modules can run 1600 MHz at less than 1.6 V. For *Typical* modules, 1400 MHz voltage requirements are between the lower 1.5 V range and 1.65 V. Most of these can do 1500 MHz at some voltage (commonly 1.7-1.8 V but sometimes as low as the 1.6 V range) and few reach 1600 MHz (usually requiring 1.8+ V if so). For *Good* modules, 1400 MHz voltage requirements can be in the lower 1.3 V range for the best modules, but more commonly in the 1.4 V range. 1500 MHz increases this to around 1.4 V for the absolute best modules and 1.50–1.61 V for most modules.

Timings also vary quite significantly depending on the module strength. tCAS strength is fairly strongly correlated with frequency strength, while tRCD and tRP are still correlated with frequency and tCAS strength, but not as strongly. For *Typical* modules, 1200 MHz CL 10 voltage requirements are between 1.60 and 1.72 V, with 1400 MHz CL 11 voltage requirements between 1.70 and close to 1.9 V. *Good* modules are below 1.60 V and 1.70 V for these, respectively, with the absolute best modules having 1200 MHz CL 10 voltage requirements approaching 1.40 V and 1400 MHz CL 11 voltage requirements of around 1.50 V. *Trash* modules can have 1200 MHz CL 10 voltage requirements nearing 1.9 V. tCAS scaling is ideal until around 1.7 V and gets progressively slightly weaker at higher voltages.

tRCD varies between 11 and 13 at 1200 MHz, with tRP ranging from 10 to 12. tRCD 13 at 1400 MHz is above average, while tRCD 11 at 1200 MHz would be good and tRCD 13 at 1466 MHz

really good. For tRP, the criteria are similar, only 1 tick lower at each of the frequencies. These criteria are for a voltage of 1.65 V, though voltage doesn't have much of an impact. tRCD voltage scaling is very minimal, while tRP scales slightly more, though both get progressively worse the higher the voltage gets. tRP may scale at 2 ns/V or better at really low voltages, dropping to ~1.3 ns/V around 1.60 V, ~0.7 ns/V in the 1.8 V range and not scaling noticeable above 2.0 V. Strength category or XMP bin doesn't have as much of an impact on tRCD and tRP as on tCAS and frequency; there are DDR3-2800 XMP modules that need tRCD 14 and tRP 13 at 1400 MHz, while some "typical strength" modules of for example DDR3-2400 XMPs can do tRCD 11 and tRP 10 at 1200 MHz. With that said, "good strength" modules are on average better than "typical strength" modules, which are in turn on average better than "trash strength" modules, and it is really only in the outliers that they cross over in tRCD and tRP strength.

As with other Hynix ICs, MFR can run tRAS equal to tRCD, or potentially lower if the platform allows it. MFR is unique among 4 Gbit Hynix ICs in that it can run tRRD 4 (and tFAW 16) at high frequencies of 1200 MHz and more, while others need 5 or 6. tRFC is rather high, commonly between 220 and 240 at 1200 MHz (183–200 ns). No or even slight negative tRFC voltage scaling above 1.65 V. These tRRD and tRFC properties can be used to reliably distinguish it from other 4 Gbit Hynix ICs, for example on Kingston modules; if tRRD 4 at 1200+ MHz is stable and 210 tRFC at 1200 MHz does not POST, it should be MFR.

4 Gbit AFR

Common on 4 Gbit-based OEM modules from 2013 and the first half of 2014. Most Corsair Vengeance Pro and Kingston HyperX 2400 11-13-13 modules from late 2013 and most of 2014 are based on these. Also used on lower speed modules from various manufacturers.

Double sided modules will typically not run more than 1200–1300 MHz. Increasing voltage to 1.70-1.85 V may help stabilizing 1300 MHz, though it is generally easier to simply target 1200 MHz. Single sided modules may run 1466 MHz and higher.

Typical tCAS would be 10–11 at 1200 MHz depending on module quality. Good modules can run tCAS 10 at around 1.5 V, with average ones requiring over 1.6 V and bad ones limited to tCAS 11 at under 1.7 V. Scaling is ideal up to the mid 1.7 V range, beyond which it gets slightly worse the higher the voltage gets.

Typical tRCD would be 13–14 and typical tRP 12–13. Modules with DDR3-2400 11-13-13 XMPs seem to consistently do better tRCD and tRP than lower bins, which makes sense. tRCD and tRP only scale minimally with voltage. tRAS can typically run the same as or slightly higher than tRCD. tRFC is among the lowest for 4 Gbit ICs, running 188-201 at 1200 MHz (156–167 ns), while tRRD is conversely among the highest for 4 Gbit ICs, usually requiring 6 at 1200 MHz and occasionally running 5.

2E0C3CA696260EA285966AA7768EA3CF63C8B3CDAC15E796C46610209AE8E1A9

Slight temperature sensitivity. Passive compared to active cooling in ambient air (25 °C) only required a 10 mV voltage increase. Additional heating with a space heater (close to 60 °C) required an additional 20 mV for equal stability. May not run 65k tREFI even at higher frequencies if very poorly cooled. Should be stable even at low frequencies with good cooling.

4 Gbit BFR

4 Gbit BFR started replacing AFR on OEM modules during late 2014. Used on a lot of DDR3-1866 and 2400 modules from 2014 and later, as well as various standard 1600 and 1333 modules. Still used on Corsair DDR3 modules in 2022, seemingly making up the majority of them.

Single rank OEM modules and some third party ones run 1466+ MHz without issue. On dual rank modules, PCB and IMC sometimes contribute to lower max clocks of 1300-1400 MHz. Many samples with 6-layer PCBs will either hit limits themselves at these clocks, or hit IMC limits despite the same IMC running 1466+ MHz on other BFR modules.

tCAS performance is similar to AFR, though BFR is seemingly slightly stronger on average at around 1.6 V. Typical timings would be 10-12-13 at 1.5–1.7 V depending on how good the module is. Some may require 1 tick higher tRCD, tRP or both. Minimum tCAS scales well with voltage, though not quite ideally. Scaling is good until around 1.8 V, above which it gets progressively worse. tRCD and tRP both scale quite well for a 4 Gbit IC, at approximately 2.5 ns/V from 1.45 V to 1.65 V with lesser scaling at higher voltages. In practice, you might be able to stabilize a somewhat unstable tRCD or tRP value with voltage, but increasing voltage won’t allow you to drop it a full tick.

Requires tRRD 5 at 1200 MHz. tRFC varies between 202 and 220 (168–183 ns). Like on other Hynix ICs, tRAS can run very low values, usually the same as or a few ticks above tRCD. tREFI seems to vary quite a bit from batch to batch. Some samples will not run 65k tREFI even at higher frequencies if poorly cooled; with good cooling, it should be stable at low frequencies.

4 Gbit DFR

Used on some third party modules from 2015 to 2017. Also used on some OEM modules. Generally quite rare.

Frequency on 8 GB modules maxes out at 1200–1333 MHz, with voltage having no impact on frequency unless dropping down to 1.3 V and lower. It is not known if frequency characteristics would be different for 4 GB modules. Timings are similar to 4 Gbit AFR. For Corsair DDR3-2400 11-13-13 modules, tRCD and tRP have both been 12–13 at 1200 MHz, though it is

possible that modules that aren't required to meet that XMP spec would need higher tRCD or tRP. tRCD is typically a bit looser than tRP, though less than a full tick on average. tCAS 10 at the same frequency has required between 1.5 and 1.7 V.

tCAS voltage scaling is almost ideal up to 1.8 V, with poor scaling at higher voltages. tRCD scales at approximately 0.9 ns/V between 1.3 and 1.8 V, with scaling dropping very slightly throughout that range. At higher voltages, scaling decreases significantly. tRP scaling is quite significant below 1.4 V, at 2 ns/V and higher. However, above 1.5 V it drops to next to nothing, but does continue to scale above 2 V. As with most Hynix, tRAS can run equal to or slightly higher than tRCD. Requires 5 tRRD at 1200 MHz. tRFC is around 200 ticks at 1200 MHz 1.65 V (166 ns), with somewhat significant scaling at lower voltages and slight rollover above 1.8 V. tWRWR scales slightly with voltage and setting it to 5 (instead of 4 at auto) may help drop the frequency voltage requirements slightly at 1200 MHz and below.

Samsung

1 Gbit C-die

Very early DDR3 IC that you're unlikely to find unless you specifically hunt for it.

Frequency voltage requirements are very high, with 800 MHz having voltage requirements around 1.4 V, 900 MHz in the 1.5 V range and 1000 MHz in the 1.7 V range. It is not especially voltage tolerant, with one sample having a maximum stable voltage of 1.88 V and another 1.99 V. At 800 MHz, expect 8-8-7 or 8-9-7 in the 1.5 V range, with tRAS running equal to or slightly higher than tRCD. tCAS scales well up to the maximum stable voltage. tRP has some slight positive scaling up to 1.7–1.8 V, after which it scales negatively somewhat. tRCD scaling is less consistent. Some samples may have some slight scaling, and mostly at below 1.5 V if so. Expect around 50 tRFC at 800 MHz 1.65 V, with some scaling with voltage.

1 Gbit D-die

Since people for some reason won't stop asking about this useless IC, HERE, I'VE FINALLY ADDED IT! Don't buy it. It pretty much only appears on higher bin modules from 2008, sucks for both timings and frequency unless at way above 2 V, and still does worse timings than Micron ICs like D9GTx and D9JNx at these high voltages.

1 Gbit E-die

Only seen on Samsung OEM modules. Some samples are quite impressive, with one tested sample doing 1400 MHz 9-14-12 at 2.0 V, which aside from tRCD is comparable to 1 Gbit G-die and 2 Gbit D-die. However, most samples are not this good and would max out a bit lower for frequency, usually with worse absolute tCAS latency, even if tRCD is similar. tRFC is around 65 ns, eg. 78 ticks at 1200 MHz.

1 Gbit F-die

Seems to only appear on OEM modules. Max frequency is between 1066 and 1333 MHz. Timings are not that impressive. At 1200 MHz, 10-12-12 or tRP 11 would be typical for 1.65 V. There are many better options for 1 Gbit ICs.

1 Gbit G-die

Late 1 Gbit IC that is only reliably found in Samsung OEM modules with corresponding part numbers. Occasionally occurs in low and standard bin third party modules from the mid to late DDR3 era.

Most modules would be expected to do 1400 MHz 9-12-13 with enough voltage. More info to come once I finish testing my collection of them.

2 Gbit B-die

Only seen on OEM modules from 2009 and early 2010.

Has a very high voltage floor, which increases only very slightly with higher frequencies, up to ~1.8 V. In other words, low voltage operation on these will require very low clocks. Seems to hit 1300–1333 MHz consistently given sufficient voltage. At 1200 MHz, expect 10-13-12-14 timings at around 1.6 V.

tCAS voltage scaling is ideal at around 1.7 V and lower, and only gets slightly worse when approaching 2 V. tRCD does not scale at all and tRP even scales very slightly negatively with voltage. tRFC is rather typical, requiring approximately 100 ns, and does not scale notably with voltage. CWL 6 was needed at 1200 MHz unless running high voltages. Do note that maximum supported CL is 11 and maximum CWL is 8, so be careful to not set them too high.

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2 Gbit C-die

Common on earlier 4 GB Samsung OEM modules using 2 Gbit ICs. Later 4 GB OEM modules typically use 4 Gbit ICs. Also sometimes found on 2 GB modules, before the switch to D-die. I have not encountered C-die on third party modules.

Frequency generally tops out somewhere between 1200 MHz and 1400 MHz, though most modules won't run 1300+ MHz and very few run 1400 MHz. CL 10 at 1200 MHz would typically require voltages in the 1.5 V range or sometimes lower, while CL 9 would need 1.65 V or more. However, some modules seem to be unable to stabilize at specifically CL 10 at 1200 MHz, which would either require pushing higher voltages for CL 9, or dropping CL to 11. tCAS scales well with voltage at a near linearly ideal relation.

Minimum tRCD and tRP values at 1200 MHz would typically be 12 for both or in some cases 11 for tRP. Linear scaling with higher frequencies. tRCD and tRP do scale very slightly with voltage, but nowhere near as much as tCAS.

Tested on two banks of 4 modules each, one bank required 40 mV more voltage for the same tCAS going from ~30 °C to 74 °C, while the other bank required 60 mV more going from ~30 °C to 81 °C. Based on this, the IC doesn't seem especially temperature sensitive, though they did easily climb to these temperatures, suggesting that they are not particularly efficient or cool-running.

2 Gbit D-die

Exclusively used on 4 GB DDR3-2666/2600 CL10, DDR3-2400 9-11-11 and DDR3-2133 CL9 1.5 V. Very common on kits with tighter absolute tCAS, such as DDR3-1600 7-8-8, 8-8-8 and 1866 8-9-9. Sometimes also found on 2133 CL9 1.65 V and 2600/2666 CL11. Used on Samsung OEM modules from 2011 to 2013.

Frequency

Frequency on D-die is quite variable. At the bottom end, some sticks won't go above 1100 MHz no matter the voltage, while good sticks can do 1400 MHz below 1.65 V and 1466+ MHz below 1.80 V. All DDR3-2400+ XMP sticks can be expected to reach 1400 MHz at some voltage. For some, this may be above 1.8 V or even approaching 2.0 V, while for others it'll be below 1.65 V. DDR3-2133 XMP sticks and other sticks of similar quality can often be as good as 2400+ sticks, but tend to be worse at the low end. For DDR3-1866 and lower XMP or OEM sticks of similar quality to these third party bins, 1200-1300 MHz maximum is typical, at least without pushing higher voltages (above 1.7-1.8 V).

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On better sticks, frequency scales with voltage notably to above 2 V. 1200 MHz will typically have frequency voltage requirements of 1.37-1.48 V. 1333 MHz is generally around 150 mV higher, giving a typical range of 1.50-1.65 V for good bin sticks.

At 1400 MHz and above, frequency voltage requirements start getting a lot more complicated. Some sticks will be fine with only a bit more than 100 mV more compared to at 1333 MHz, while others may need over 300 mV more. Adding to this variability in scaling, timing tightness also impacts the frequency voltage requirements rather significantly on many samples when at above 1333 MHz. The effect is the opposite of what may be expected, where tighter timings tend to reduce the frequency voltage requirements. This seems most prominent for second timings, but also applies to first timings, most notably CL. It has not been identified whether or not it is a single second timing or a combination of multiple that serve to increase the frequency voltage requirements when loose.

How big the impact of tight timings is on the frequency voltage requirement varies from sample to sample. Some samples may see over a 200 mV reduction in frequency voltage requirements at 1400+ MHz while others may only benefit 10-30 mV. Worth noting however is that I have not observed any samples benefitting from looser second timings beyond tight-but-safe values. Third timings like tRDRD, tWRWR and tRDWR do not appear to negatively impact the frequency voltage requirement. In some cases, tightening tRDRD and tWRWR fully can have slightly higher voltage requirements than the frequency voltage requirements with them loose.

Some samples will have a maximum stable voltage that scales negatively with increased frequency when close to the frequency limit. For example, one sample may be fine at 2.4 V at 1440 MHz, but unstable above 2.2 V at 1466 MHz. Sometimes these maximum voltage limits are imposed by tRDRD or tWRWR (assuming tRDRD 5 and tWRWR 4 are used as a baseline) rather than the frequency itself, in which case loosening them can help increase the maximum stable voltage at high frequency. Generally, memory maximum frequency limits (whether by fundamental frequency or tRDRD/tWRWR) are more prominent in memory tests than 32M.

tCAS

tCAS is simple to bin on D-die. It can be expected to scale well with voltage on all samples until potential voltage limits imposed by other factors (like frequency or tRDRD/tWRWR max voltages). 1200 MHz CL 9 voltage requirements can be used to compare all but the absolute worst modules (the 1/50 samples that can't do 1200 MHz). Top bin modules (2400 9-11-11 and 2600/2666 10-12-12 XMP) have 1200 MHz CL 9 voltage requirements between 1.50 and 1.60 V. Some modules from looser XMPs such as 2400 10-12-12 and 2666 11-13-13 as well as certain OEM modules will also be in this range. I have not observed any DDR3-2133 and lower XMP modules having 1200 MHz CL 9 voltage requirements lower than 1.60 V. DDR3-2133 CL 9 XMP and worse DDR4-2400 10-12-12 or 2666 11-13-13 XMP modules tend to have voltage

requirements between 1.60 and 1.70 V. DDR3-2133 XMP modules looser than CL 9 can have a bit higher voltage requirements, but usually don't go much above 1.70 V. Lower bin XMP modules and worse OEM modules can be expected to all need above 1.7 V and potentially above 1.8 V.

For these lower voltages, the choice of test does not make a big difference to voltage requirements. At higher voltages, the differences become more significant. At around 2.0 V for 1400 MHz CL 9, the difference between minimum 32M and memory test voltage is typically around 50 mV. This grows to around 100 mV at around 2.2 V and we would expect the gap to increase even more at even higher voltages.

For 1400 MHz CL 9, everything with voltage requirements of around 2.0 V or lower should be sufficient to not be limited by tCAS strength for most benching use cases. When comparing memory test voltage requirements, modules with 1200 MHz CL 9 voltage requirements of 1.57 V will usually need 2.01 V for 1400 MHz CL 9. Modules with 1200 MHz CL 9 voltage requirements of 1.65 V will commonly need 2.25 V for 1400 MHz CL 9. Switching to 32M instead brings this down closer to 2.15 V which still allows for reasonable headroom for pushing higher CL 9 frequency, even on motherboards with only a 2.4 V voltage limit.

tRCD/tRP

tRCD and tRP only scale minimally with voltage. At a tick value of 11 or 12, going from 1.65 V to 2.05 V typically gains 40-50 MHz of maximum frequency on both. 2.05 V to 2.40 V is a bit more variable with gains between 15 and 30 MHz. Some sticks have anomalous tRP voltage scaling behavior where they scale significantly worse than above-given figures, sometimes to the extent of not scaling at all or even negatively. Typically, this is more prominent in memory tests than 32M.

The two timings are quite evenly matched on average. tRP is most commonly the stronger of the two, though some modules are stronger on tRCD than tRP. Generally, since the difference between them is so minor, one wants to target running them equal. This means that the weaker one will be what imposes frequency limits at given tRCD/tRP tick values.

Good modules will do 1330+ MHz at around 2.0 V and 1350+ MHz at 2.4 V. This should for reference be good enough for 1466 MHz tRCD/tRP 12. Worse modules have tRCD/tRP 11 limits maxing out around 1300 MHz at 2.4 V or once again around 20 MHz lower at 2.0 V. This is still sufficient for 1400 MHz tRCD/tRP 12, but not much more. The absolute worst modules can have tRCD or tRP 11 maxing out at around 1250 MHz for 2.4 V or a bit below 1200 MHz for 1.65 V.

Other timings

tRAS of 1-2 ticks higher than minimized tRCD/tRP is usually required. Some sticks will run tRAS equal to tRCD/tRP at certain frequencies, but this is not the norm.

Expect around 73 ns tRFC for good modules, translating to a bit under 90 ticks at 1200 MHz, 102 ticks at 1400 MHz or 108 at 1466 MHz. The worst modules are closer to 83 ns, or a bit under 100 ticks at 1200 MHz. tRFC voltage scaling is minimal. Even just a 1 tick drop requires a few hundred mV.

Typical tRDRD/tWRWR is 5/4 for frequencies of ~1300 MHz and above. Some modules are able to do tRDRD 4 at 1333 MHz, though tRDRD 4 at 1400 MHz is not known to be possible. Loosening one, either or both of tRDRD and tWRWR can sometimes help at high frequencies, though this is arguably not worth it due to the performance loss it incurs, especially for tRDRD.

For the remaining timings, the following should work on most modules:
tRRD 4, tFAW 16, tRTP 4, tWR 5, CWL 5, tWTR 5

Personally, I increase tWR, CWL and tWTR to 6 when just binning for some added margin.

Note that 1150 motherboards report tWTR 2 lower than it actually is.

I have not found tight subtimings to have much of an impact on tCAS voltage requirements, but due to reasons mentioned in the frequency section above, I recommend always testing with them tight.

Limits when pushing maximum 9-12-12 frequency

For modules with 1400 MHz CL 9 voltage requirements of around 2.0 V or lower, tCAS strength should not be much of a limit for maximum 9-12-12 frequency. For modules with 1400 MHz CL 9 voltage requirements above 2.1 V and especially above 2.2 V, tCAS strength starts becoming more of a concern. This is particularly the case if limited to 2.4 V by the motherboard. Effectively, this means that tCAS strength for modules of 2400 9-11-11 and 2600/2666 10-12-12 bins should not be a concern for 9-12-12 frequency, as all such modules should be guaranteed sufficiently strong tCAS by the XMP spec.

Fundamental frequency limits are another concern which may limit max 9-12-12 frequency. As discussed, frequency voltage requirements are highly variable, even among top bins. While modules with 1400 MHz frequency voltage requirements below 1.8 V should be able to run 1466+ MHz at higher voltage assuming reasonable scaling, this may not be the case for modules with 1400 MHz frequency voltage requirements above 1.8 V. Lower bin modules may not even

hit 1400 MHz to begin with, though tCAS and tRCD/tRP strength tends to be poor on these anyways.

The most common limit for the higher XMP bins is tRCD/tRP strength. Even getting enough tRCD/tRP strength for 1450 MHz 9-12-12 is not the most common. For 1466 MHz, it is rather rare. tRCD and tRP strong enough for more than 1466 MHz 9-12-12 is very rare.

Maximum voltage limits at high frequency are another potential limiting factor, especially for 9-12-12 frequency in memory tests. Some modules may be unable to tolerate above as low as 2.1 V at 1466 MHz, which would require unrealistically low tCAS voltage requirements for CL 9 to be possible. Looser tRDRD or tWRWR may help with max voltage at high frequency, though with a hit to performance and therefore questionable practicality.

“2” Gbit Q-die (P-die)

Mostly present in certain third party modules from 2014 and 2015. Found in what is supposedly a GDDR3 package, labeled as K4W2G0846P-HC15 (which would normally indicate “P-die”). These were likely intended for use on low-end GPUs such as GT 730s, but must not have been as popular as expected, given that they found their way to standard DDR3 modules.

For characteristics besides tRFC, see 4 Gbit Q-die. It seems apparent that this IC is simply a density downbin of it, likely for samples with faults making the full capacity unusable. As is natural with density downbins, this brings lower tRFC compared to the full density version. For the 2 Gbit version, this is some of the worst of 2 Gbit ICs at around 125 ns.

2 Gbit E-die

Appears on some later (2014+) OEM modules. Probably mainly on 2 GB single sided ones, as 4 GB modules had primarily moved to 4 Gbit ICs by this point. Seems similar to “2 Gbit” Q-die above.

2 Gbit F-die

Very rare IC. Only spotted on a Transcend OEM module from 2018. The following results are based on testing of that (single) module.

Very impressive IC, reaching 1500 MHz easily and only needing 1.42 V for it. Likely to go significantly higher with more voltage as well. Perhaps the most impressive thing however is the

ability to run tCCD 4 without increased voltage up to the maximum tested frequency of 1500 MHz, meaning that you don't have to make any performance trade offs to run high frequency.

Timings aren't anything all that special, with the tested sample running 11-12-11 at 1200 MHz 1.51 V. tCAS keeps scaling well to over 2 V, making it possible to run CL 8 at 2.18 V. tRCD on the other hand only scales positively at very low voltages and starts scaling negatively above ~1.35 V, losing 1.0 ns (1040 to 940 MHz max at tRCD 10) going from 1.4 to 2.2 V. tRP has slight positive scaling throughout the entire voltage range, but it is very minimal at higher voltages, only gaining 0.12 ns (1040 to 1055 MHz max at tRP 9) between 1.8 and 2.4 V.

tRAS should not need to be more than a few ticks higher than tRCD. tRRD has some slight negative scaling and 5 was needed for above 1.35 V at 1200 MHz, while 4 was stable at and below 1.35 V. However, for 1466 MHz, 5 was stable across the full voltage range. tRFC is around 141 ticks at 1200 MHz (~117 ns) 1.65 V, losing a few ticks when dropping to 1.2 V and gaining a few ticks up to the maximum tested voltage of 2.4 V. CWL may need to be greater than 5 at below 1.5 V at 1200 MHz or at higher frequencies even with higher voltage.

2 Gbit S-die

Unlikely to be found on anything unless specifically looking for it. Seems to be most common on 2 GB modules of basic XMPs or JEDEC specs from around 2015.

Maximum stable voltage decreases as frequency is increased, while the frequency voltage requirement increases. The optimal voltage for frequency will be where the two converge, which seems to be in the 1.5 V range. For full stability, 1400 MHz was the maximum on two tested samples. Going from 1.65 V or a bit lower to 2+ V might drop maximum frequency to 1200 MHz. Of note is that tRDRD 4 was possible at 1400 MHz, which should make it a fair bit faster than the same frequency on other ICs that require tRDRD 5.

Timings are unremarkable. At 1200 MHz, expect 11-13-12-13 timings at 1.65 V. tCAS scales to at least 2.0 V, though not especially well. Although tRCD scales ideally at extremely low voltages (<1.2 V), neither tRCD nor tRP seem to scale reliably or at all above 1.4 V. tRFC is the worst of all the 2 Gbit ICs I've tested, requiring 168 ticks at 1200 MHz (140 ns) and not scaling notably with voltage above 1.35 V.

4 Gbit B-die

Found on various 8 GB modules with tight CL/f XMPs manufactured during 2012 and 2013, such as DDR3-1600 CL7, 2133 CL9 and 2400 10-12-12. Used on Samsung 4 Gbit OEM modules during 2012 and 2013, with later modules using D-, E- or Q-die.

Maximum frequency scales negatively with both voltage and temperature. 1200 MHz is typically stable with active cooling, often at up to ~1.8 V, while it might be unachievable or require voltages lower than 1.5 V without a fan, depending on the sample. Some tested modules have lost over 50 MHz going from active to passive cooling.

tCAS 10 at 1200 MHz will typically require a voltage between 1.45 V and 1.60 V depending on the module. tCAS scales well with voltage but not perfectly linearly. Some insane modules will run 1200 MHz CL9 at around 1.5 V (CMD64GX3M8A2400C10 in my case). While tCAS does scale reasonably well up to 1.9 V, the negative frequency scaling will likely limit your maximum voltage before then unless running at 1066 MHz and lower.

Typical tRCD and tRP at 1200 MHz would be 10 and 12 respectively. Voltage only has a minimal impact on tRCD and tRP. The tRCD variation between different modules is minimal. tRP is usually also very consistent, but some modules will be able to run it one tick lower.

4 Gbit Q-die

Used on various 8 GB third party modules produced from 2014 until recently, which is curious since Q-die production ceased many years ago. Seems especially common on DDR3-2133 11-11-11 modules. Also used on lower speed modules such as DDR3-1600 from the later DDR3 era. Sometimes found on OEM-modules, but D-die seems a lot more common.

Frequency characteristics are very similar to B-die. 1200 MHz can generally be expected to be the limit. Good cooling has a big impact on maximum stable frequency, with some modules losing 100 MHz stable frequency going from optimal cooling to very poor cooling. Maximum stable frequency also scales negatively with voltage, with one strong (for frequency) module being moderately unstable at 1300 MHz with 1.65 V, but barely stable at 1400 MHz with 1.30 V. As a result of this, the voltage may need to be dropped to around 1.5 V to maintain stability at 1200 MHz with poor cooling.

tCAS performance is also very similar to B-die. Q-die seems to require slightly higher voltage on average for the same tCAS. As with B-die, negative frequency scaling will likely limit your maximum voltage unless running at low frequencies. Typical tRCD would be 12 at 1200 MHz. tRP will vary, with some modules requiring 12 at 1200 MHz and some going as low as 10. Requires tRAS of around 14 ns, or 16 ticks at 1200 MHz. tRCD scales at roughly 1.0 ns/V up to around 1.7 V, with significantly worse scaling at higher voltages. tRP scaling is closer to 0.5 ns/V. Requires tRFC of between 230 and 245 at 1200 MHz (~200 ns), with scaling of approximately 1 tick per 150 mV, tested from 1.35 V to 1.80 V. tRRD should run 4 at 1200 MHz on most samples.

4 Gbit D-die

Very common on Samsung OEM modules from 2014 onwards. Sometimes also used in third party modules with standard XMP profiles such as DDR3-1600 9-9-9 from the same time period.

Most modules would be expected to hit 1400 or 1466 MHz with the voltage tuned for frequency. The minimum voltage requirement is fairly low for these, and doesn't increase much with frequency, commonly ~1.20 V at 1200 MHz and ~1.37 V at 1466 MHz. Frequency also scales negatively with voltage, into at least the 1.4 V range. Consequently, the maximum frequency will be achieved where the minimum and maximum frequency voltages converge, which would be expected in the 1.4–1.6 V range, mostly depending on how tolerant the sample is of higher voltages.

At 1200 MHz, 11-13-12-13 timings would be expected at 1.52–1.72 V, with some samples requiring one tick higher of one or multiple of the non-tCAS timings. tCAS voltage scaling in the standard and high voltage range is not great, typically requiring a bit more than 300 mV higher voltage for CL 10, which is about 2/3 of ideal scaling. In some rough testing in the standard and high voltage ranges, it seems like tRCD may roll over slightly while tRP scales very slightly.

While the IC does support CL 15, it does not support above CWL 10, which may require you to set CWL manually to get CL 15 working. On samples weak in tCAS or max voltage for frequency, this may be required to reach the maximum clock potential. tRFC is a bit worse than average for 4 Gbit ICs, at roughly 190 ns. tRRD may need to be higher than 4 at higher frequencies (1200+ MHz).

4 Gbit E-die

Only found on Samsung OEM modules from 2015 onwards.

Generally like a better version of D-die. Maximum frequency is usually well above 1466 MHz for most samples, but some samples clock worse. No apparent negative frequency scaling at high voltage. Typical timings at 1200 MHz would be 10-13-12 at 1.48–1.75 V. tCAS scales with voltage up to at least 2.1 V, though scaling isn’t great even at lower voltages, and gets very poor at high voltage, with less than half of ideal voltage scaling. tRAS usually needs to be a few ticks above tRCD. Runs low tRFC for 4 Gbit ICs, at around 160 ns. May need 5 tRRD at 1200 MHz.

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Micron

1 Gbit B-die/V48A (D9GTR, GTS, GTX, GTN)

Found on some very early (2007–2008) kits rated for fairly low timings at high voltages, with speeds commonly between 800 and 1000 MHz.

All three primary timings scale well with voltage to well beyond 2 V. For better modules, expect 7-6-6 or 7-7-6 timings at 1000+ MHz with 2.1 V or more. Usually needs high voltages to be able to reach higher clocks. Some samples may not even do 900 MHz if trying to stick to lower voltages. For more typical modules, expect to need CL 8.

1 Gbit D-die/V48C (D9JNL, D9JNM)

Used on all sorts of OCZ, from garbage bins like DDR3-1333 9-9-9 1.70 V to seemingly good bins like 1600 7-6-6 and 2000 9-9-9. Used in Corsair ver 3.2 with 2008 and 2009 date code.

Somewhat similar to D9GTx above, but generally worse in all aspects. Frequency scales well with voltage, and is quite variable in general. Some D9JNL requires above 1.6 V for 666 MHz, while good D9JNM may go beyond 1000 MHz at 1.6 V. Expect 1000 MHz 7-7-7 at around 2 V for the best samples. For full memory test stability, maximum stable voltage is usually between 2.0 and 2.2 V. For lighter loads like SuperPi 32M, the maximum stable voltage goes even higher, especially if running maxmem. This makes the IC an acceptable budget benching alternative for lower clock platforms since even more average samples can often be made to do 1000 MHz 7-7-7 in maxmem 32M with enough voltage.

1 Gbit F-die/V58B (D9KPT)

Found in various OCZ kits, some of seemingly impressive bins like DDR3-1600 7-7-7 1.65 V. Corsair ver 3.1 with 2009–2010 date codes. Also used on Micron OEM modules.

Clocks better than D-die above, and doesn’t require high voltage for frequency to the same extent. Most samples should run 1100 MHz, and some will run 1200+ MHz.

Timings aren’t all that special. Expect 1000 MHz 8-8-7 at best. Some samples don’t tolerate voltage well and become unstable as low as 1.76 V, while others scale to closer to 2 V. These are generally more consistent than the previous two Micron IC, so an average sample may in fact be better, even if good samples of B and D-die beat it.

1 Gbit G-die/V68A (D9MNL)

Mostly used on Micron OEM modules. May rarely appear in third party modules (possibly Corsair ver 3.7).

Maximum frequency is usually around 1000 MHz, with the best samples reaching 1100 MHz. Expect ~10 ns tCAS and tRCD, with slightly lower tRP. Voltage scaling is poor.

2 Gbit A-die/V49A (D9KLV)

Seems to only be used on early 4 GB Micron OEM modules from 2009 or early 2010. One thing to note is that these ICs are massive, and on a fully populated ECC DIMM, they take up almost the entire PCB area.

As tested on 4 unbinned OEM samples, they are similar to D9JNL in most regards. High voltage is required for any reasonable clocks. Expect to hit 1000 MHz with enough voltage, usually around 1.7 V. tCAS and tRCD scale ideally or better than ideally with voltage, while tRP does not scale at all. tRAS and tRFC also scale slightly.

At 1000 MHz, expect 8-8-8-20-80 timings with around 1.9 V. If these were to be binned on the same scale as D9JNx, good samples would likely be able to do 7-7-7 at around 2.0 V.

Do note that maximum supported CL is 11, and maximum supported CWL is 8 (usually auto at CL 11). This should not be a limiting factor since frequency will be the voltage limit before maximum CL, but it is still worth keeping in mind to prevent running into issues due to CL set too high.

2 Gbit D-die/V69A (D9LGK, LGL, KRT)

These are found on early 4 GB Micron OEM modules. Likely also used on some or many of the early 4 GB third party modules with poor overclocking characteristics, but I haven't been tempted to delid such modules to confirm.

Avoid for overclocking. Typically don't like running above 800 MHz. Many modules of lower speed bins won't even run 800 MHz with full stability. 10-8-8 timings with high tRAS would be typical at 800 MHz. Very little if any voltage scaling. Only interesting thing about them is the somewhat low tRFC, which isn’t very useful on an IC that is otherwise garbage.

2 Gbit H-die/V79B

Rather uncommon. Used in some rare Micron OEM modules, Corsair ver 3.17 and occasional earlier Crucial 4 GB modules.

Expect 1000 MHz. Some samples will reach 1100 MHz. Timings are poor. Standard modules run 12-12-10 at 1000–1100 MHz with inconsistent voltage scaling, while some good Crucial bins can run flat 10s.

2 Gbit M-die/V79D (D9PFJ, PFW, PXF)

There are also some older 2011 BGA codes that indicate M-die, but I am unable to recall them.

Found on various third party modules based on Micron ICs from 2011 to 2013. Used on OEM modules from 2011 and 2012. Corsair ver 3.19, though uncommon.

There are two main variants of this IC: D9 (usually D9PFJ) and the special Crucial/SpecTek variant. The special Crucial/SpecTek variant is found on Crucial modules with the 1600 8-8-8 and 1866 9-9-9 specs, while the SpecTek variant is sometimes found on Corsair ver 3.19 (though this can also be just standard D9PFJ). For the standard D9 variant, I refer readers to Nanya 2 Gbit G-die, as these have the same characteristics and are likely the same IC design.

The special Crucial/SpecTek variant usually maxes out somewhere between 1100 and a bit over 1200 MHz. Some modules feature early-onset negative-frequency-scaling max voltages. What this means is that they may as an example be able to take above 1.8 V at 1000 MHz, while 1100 MHz maxes out in the 1.6 V range and 1200 MHz at around 1.5 V. This property, if present, will limit timings at higher frequencies since low voltage will be required. Note however that only a minority of modules have this property.

1200 MHz 9-x-9 usually requires around 1.7 V or a bit more. On some modules, tRCD will run at 9 with no extra voltage required, while on others you will either need to run 10 or increase voltage for tRCD 9. tCAS and tRP scale well to higher voltage if not hitting the early-onset negative-frequency-scaling max voltage. tRCD also scales, but not quite as well as tCAS and tRP. It is not that uncommon to get modules that will do 1200 MHz 8-8-8 or 1066 MHz 7-7-7 with enough voltage. With binning, it should be possible to get modules that will do 1200 MHz 7-8-7 and/or 1066 MHz 6-7-6, though at well over 2 V.

tRAS at 1200 MHz 9-x-9 is usually 22, with moderate voltage scaling. You'd therefore expect it to drop a bit at higher voltages or need to be a bit looser at lower voltages. tRFC at 1200 MHz 9-x-9 can creep below 110 ticks, though not hitting 100, giving a tRFC of around 90 ns. It also scales moderately with voltage.

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2 Gbit K-die/V89C (D9PSH, PSF, QMS, PXF)

Despite the lower die revision (though higher design ID), these are supposedly newer than V79D and are still in production according to Micron's product site. I have seen them on some OEM modules and they are also used on some newer (2014+ ?) Crucial modules. Possibly used in other third party modules as well. They generally appear to be rare though.

These are generally similar to the above V79D. There are two main variants of it: the standard D9 variant which is likely the same IC design as Nanya 2 Gbit F-die, and the special Crucial variant found on Crucial 1600 8-8-8 and 1866 9-9-9 modules. I have not seen any evidence of a special SpecTek variant, like for V79D on some Corsair ver 3.19 modules. See Nanya F-die for characteristics of the D9 variant. The special Crucial variant appears similar to the special variant of V79D based on my limited sample size.

4 Gbit D-die/V70S (D9PCP, NZZ, QFG)

Extremely rare. Seems to only appear in very early low or even JEDEC bin 8 GB modules. Likely also used on some early (2012) high density Micron modules. Curiously enough, it has been spotted on a Crucial 1600 8-8-8 kit.

Maximum frequency around 1000 MHz. Two tested samples ran 10-11-8 timings at 1.60 V at this frequency. tCAS scales to around 1.8 V in the 950–1000 MHz range, but seems to scale to 2+ V at lower frequencies. Scaling is generally poor above 1.75 V though. tRCD and tRP only scale minimally from voltage.

As with other Microns, requires high tRAS of around 22 ns. tRFC is in the lower range for 4 Gbit modules, running around 150 ns (eq. 180 ticks @ 1200 MHz).

4 Gbit E-die/V80A (D9QBJ, QBN, QBS)

Used on nearly all Micron OEM modules from 2013 until early/mid 2015. Also used on various third party modules from the same time period, mostly standard DDR3-1600 and somewhat often on 1866 and 2133 kits. Oddly enough, some of Corsair's 4 and 8 GB DDR3-2666 C11 kits are based on these. While there are no such designations officially, I like to subdivide these into 3 categories: "D9QBJ", "Corsair SpecTek PEB12" and "Crucial top bin V80A".

D9QBJ

D9QBJ, a designation that the ICs are commonly known by, is the standard Micron bin of the V80A product, sold with a full specification and validation testing. This is the IC that is found on V80A-based OEM modules from mainly Micron but also others like Ramaxel. To this tier, I also group Crucial modules of basic bins like 1600 9-9-9, even if they do not carry the D9QBJ designation.

Regardless of the exact source, ICs within this category can be expected to perform mostly the same. For double-sided modules, 1066–1100 MHz is most commonly the frequency limit, though some will hit 1200 MHz. For these modules, frequency does not scale with voltage to a significant extent. In practice, this means that 1200 MHz is usually unobtainable even when pushing higher voltages if it is not stable in the standard voltage range. In fact, some samples which are unstable above 1066 MHz at 1.65 V will not even be able to hit 1100 MHz with more voltage.

For single-sided modules, the frequency range is a lot more variable. There are once again modules which are unstable above 1066 MHz, while there are modules that easily surpass 1466 MHz without having to increase the voltage above 1.65 V. These single-sided modules generally exhibit reasonable frequency scaling with voltage, as compared to the double-sided ones. Going from 1.65 V to 1.80 V is often enough to stabilize a frequency that POSTs but is very unstable.

At 933 MHz, better modules will be able to run 8-10-9-25 in the standard voltage range, while bad ones are unstable to stabilize CL 8 at any voltage. These better modules would commonly do 10-13-12-31 timings at 1200 MHz with roughly 150 mV higher voltage than the previous 933 MHz settings. Alternatively, 1200 MHz CL 11 would drop the voltage requirement by 230–300 mV. A fair number of modules are also able to achieve tRCD 12 at 1200 MHz. For modules that can reach 1466 MHz, 13-16-15-39 timings would be typical in the standard voltage range, or 1 tick lower on each of the timings for better modules (though in this case requiring a voltage bump for the lower tCAS). Some modules feature a timing anomaly on tRP, where they may require two ticks higher tRP than in the examples given above. On these modules, the typical tRP will almost always still POST, but just not be fully stable. These modules can appear in the same batch or kit as other modules without the anomalous tRP behavior, so it is seemingly not a matter of standard batch quality variance.

Voltage scaling is rather poor across the board. tCAS scaling above 1.65 V can be less than half of ideal scaling. While it does improve slightly at lower voltages, it is still far from good. Only at below 1.4 V does it start to approach ideal scaling. tRCD and tRP voltage scaling varies a fair bit from sample to sample. On some samples, voltage has no noticeable impact on tRCD or tRP stability in the standard voltage range and higher, while on other samples it has a small but notable impact, likely close to the tRCD/tRP voltage scaling on 4 Gbit BFR. tRAS (effectively tRC) scales more reliably than tRCD and tRP, often reducing by one tick with a significant (very

roughly 200 mV) voltage increase. tRFC also scales somewhat with voltage, with typical values being 165–185 ns depending on the sample. Maximum voltage regardless of timings seems to be anywhere between ~2.0 V and 2.2 V, depending on the sample. With that said, it is possible that above 2.0-2.1 V can be damaging (see later sections); in combination with the poor voltage scaling, this means there is little practical reason to run voltages this high.

Corsair SpecTek PEB12

The second category is what I refer to as Corsair SpecTek PEB12. As the name suggests, these are found on Corsair modules, specifically with version number 3.24. While standard D9QBJ can also appear on Corsair ver 3.24 (seemingly mainly on 2012 modules), it is rare in comparison. These ICs are sold through SpecTek, which is a secondary Micron supply channel. Here, PEB12 is the SpecTek mark code for Micron's V80A product. While officially unconfirmed, it is evident by stark difference in characteristics that these ICs are at the very least a unique first-party bin from Micron, sold through the SpecTek channel to Corsair, and possibly even distinct from standard D9QBJ on a design or manufacturing level (similar to the differences between normal 1 Gbit BASE and BASE Hyper).

Frequency characteristics generally seem to be similar to D9QBJ, with some notable differences. Compared to D9QBJ, some double-sided Corsair PEB12 is able to reach fairly high frequencies of 1400 MHz and even 1466 MHz with more voltage. This is however inconsistent, and most double-sided modules will still max out at 1066–1200 MHz. Even so, 1200 MHz seems to be a fair bit more common on double-sided Corsair PEB12 when compared to double-sided D9QBJ. Single-sided frequency behavior seems very similar to normal D9QBJ in general.

Average samples and better are commonly able to run tCAS and tRCD in the lower 8 ns range (i.e. 933 MHz 8, 1066–1100 MHz 9 and 1200 MHz 10) at between 1.45 and 1.60 V depending on the exact timing latency and sample. However, on some samples, these timings may exhibit non-linear scaling with frequency. For example, a sample that is able to run 933 MHz tRCD 8 (8.57 ns) could require tRCD 12 (10 ns) for 1200 MHz at the same or higher voltage. This non-linear scaling, if present, often gets even worse at higher frequencies, if achievable. The non-linear CL scaling is slightly different. It seems to only appear when running the highest stable frequency strap. An example of this would be how a module might run CL 9 just fine at 1100 MHz, but require CL 13 for 1200 MHz. Based on some limited testing, it appears this could partly be caused by CWL (which if left on auto changes with CL), as manually setting CWL high allowed CL to go lower. Still, some of these tested samples were not able to reach the expected CL based on linear scaling even with CWL set high.

Before getting to tRP, it is worth mentioning voltage scaling, as this ties in with tRP. tCAS and tRP both scale ideally or close to it with voltage. tRP scales ideally up to a point (which may be below typical voltages). At some higher point, which could be as low as 1.5 V and as high as

1.85 V, it starts scaling negatively. Initially, this negative scaling is fairly minimal, which means you might be able to trade 1 tick lower tCAS and tRCD for one tick higher tRP with more voltage. At above 1.9-2.0 V, the negative scaling starts to get severe, and at even higher voltages, it is simply comical. One tested sample went from 2.03 V max at tRP 17, to being stable at 2.2 V with tRP 31. In practice, this usually means the maximum sensible voltage ends up being somewhere around 1.9 V. It is possible that some samples also feature non-linear frequency scaling on tRP (as with tRCD described above), though the voltage rollover makes this harder to test. For a strong sample with high voltage tolerance for tRP, one might expect to be able to run 1200 MHz 8-8-9. 9-9-11 would be more typical on above-average samples, if 1200 MHz is achievable.

tRC (which is tRCD + tRP) varies depending on voltage and sample quality, but roughly 30 ns (36 ticks at 1200 MHz or 28 at 933 MHz) is to be expected. It scales meaningfully with voltage; with the voltage required for 1 tick lower tCAS/tRCD, you would expect to drop tRC by 1–2 ticks. Expect around 150 ns for tRFC, with moderate voltage scaling at above 1.65 V and more significant voltage scaling at lower voltages.

Crucial top bin V80A

The third bin category, "Crucial top bin V80A", is exclusively found on "high-end" Crucial kits, such as 1600 8-8-8 or 1866 9-9-9, with a part number ending in .16FER(2) or .16FED(2). In general, this bin is much the same as Corsair PEB12, with some differences. The first notable difference is that these seem to not exhibit the non-linear timing scaling sometimes present on Corsair PEB12. The second difference is that these seem unable to achieve any higher frequencies. Whether or not this is actually due to the ICs themselves or the PCBs used by Crucial is unknown. For 8 GB modules, this means a maximum frequency of 1200 MHz and sometimes 1066 or 1100 MHz. 4 GB modules based on .16FER2/.16FED2 seem to clock a bit higher, fairly consistently hitting 1300 MHz.

The “.16FER2” IC

It is worth examining these “.16FER2” (also including .16FED2) ICs in closer detail, as they are not standard 4 Gbit V80A. It appears that they are cut down to 2 Gbit capacity from 4 Gbit V80A. This was likely a way for Micron to salvage partially defective chips, since there are no major differences in characteristics between them other than tRFC (which tends to naturally change with density).

These ICs are found exclusively on Crucial modules, likely because it was easier for Micron to offload them through the Crucial channel than making a separate product, part number and

specification for them to sell to the general market. I find that they can belong to either the "D9QBJ" or "Crucial top bin" category, where the D9QBJ-style ones are found on basic bins such as DDR3-1600 9-9-9, while the top bins are once again found on bins like 1600 8-8-8 and 1866 9-9-9. For behavior and timing characteristics other than tRFC, see the respective sections above. Note as well that since these are cut down to 2 Gbit density, 4 GB modules will be double sided and thus hit similar frequency walls as 8 GB full density modules. The one notable exception is that top bin .16FER2 somewhat consistently hits 1300 MHz, which is typically not possible with full density top bin V80A. Single sided .16FER2 modules exist, but are rare, and I have not tested their characteristics. Expect 65–82 ns tRFC, where once again the top bin modules are better than basic bins. In other terms, typical tRFC for these is about 44% of the respective full density V80A variants, which puts it in line with 1 Gbit ICs. Once again, tRFC scales somewhat with voltage.

Top bin expectations and benching relevance

I would also like to quickly discuss the potential top bin relevance and expectations. So far, I have had samples capable of 1200 MHz 8-8-x and 8-9-9 independently, but not both at the same time. Furthermore, some of these 1200 MHz CL8 samples have had some voltage headroom before running into the severe adverse tRP scaling. With enough binning, I expect that both strong tRCD and tRP could be achieved on the same module, for 1200 MHz 8-8-9 ability, possibly with some voltage scaling headroom on tCAS and tRCD before requiring a tRP increase. Extrapolating this to 1400 MHz, which has proven to be possible, just not with Crucial modules (potentially due to PCB limitations), one might expect that 1400 MHz 9-9-11 or 9-10-11 would be possible. If this is done with the density cut .16FER2 IC, low tRFC would also be expected, similar to or better than 2 Gbit Samsung D-die. Based on this, I theorize that with sufficient binning (possibly on a per-IC basis) and a good PCB, highly competitive modules for benchmarking could be made from these ICs.

V80A random deaths

Lastly, it is also worth discussing the wide-spread phenomenon of V80A random deaths or failures. The Micron V80A product is widely known to have a tendency to fail, even if no such acknowledgements have officially been made by Micron to my knowledge. This affects all of the previously mentioned V80A categories, but seems to be particularly common for D9QBJ on Crucial modules. Kingston modules based on D9QBJ also seem to exhibit high failure rates, though it is unclear whether or not this can fully be attributed to V80A failures since Kingston modules have been documented to fail more often than expected with other ICs that are not known to fail. While the failures are most common on these two brands of modules, they occur

on all V80A, including OEM D9QBJ and Corsair SpecTek PEB12, though seemingly to a lower extent.

The failures mostly manifest themselves in the form of errors regardless of settings. The frequency of these errors varies, from very obvious instability with hundreds of errors per second in MemTest86, to intermittent instability with one error per 10 hours or less. I speculate that there is a lot of intermittently unstable V80A in use, based on speaking to people whom I have bought faulty V80A modules from, who claimed to have noticed no issues in normal use. Only rarely do these failures manifest themselves in fully dead (no POST) modules.

These wide-spread failures make it difficult to properly test and verify maximum safe voltages. One tested top bin Crucial sample started erroring irrespective of settings after about an hour at 2.2 V, though it cannot be said with confidence that this was due to the voltage since it could have been a natural failure occurring during testing at this high voltage. Regardless, there is little point in running voltages above 2.0 V, both on D9QBJ and good bin V80A, since D9QBJ scales very poorly at high voltages, and good bin V80A rolls over on tRP.

4 Gbit J-die/V80B

Rare. Found as SpecTek on some GOODRAM JEDEC modules. Corsair ver 3.28 and possibly 3.29. Probably most likely to be found on JEDEC modules from manufacturers known to use odd ICs.

1200 MHz tends to be on the edge of stability; some samples can barely run it while others are slightly unstable at it.. Runs poor timings of 11-13-13 at 1100 MHz in the 1.5 V range. tCAS scales quite well with voltage up to at least 2 V. No noticeable voltage scaling for tRCD and tRP. Primary timings seem to scale close to perfectly linearly with frequency.

As with other Microns, requires high tRAS of around 24 ns. tRFC is slightly high for 4 Gbit ICs, running 210 ticks at 1100 MHz. Like other Microns, some samples need very high JEDEC tWR for full stability. These will still POSTs down to the minimum configurable of 5 (compared to 12 for JEDEC), but become increasingly unstable for each tick lower.

4 Gbit N-die/V90B (D9RVX)

Popular on Micron and Kingston OEM modules from 2015 and 2016, especially the second half of 2015 onwards, when it had largely replaced D9QBJ. Not seen much on modules from other manufacturers, other than Crucial (Micron brand).

Maximum clock for single sided modules is often between 1333 and 1466 MHz, with some even going a bit higher. Timings on most modules are rather poor. At 1200 MHz, expect 12-14-11-28 for typical modules, though some top bin Crucial modules go much tighter. No timings scale significantly with voltage.

This IC has some of the lowest absolute voltage requirements for high frequency, with one sample being able to run 1400 MHz at 1.12 V and 1466 MHz at 1.27 V, given sufficiently high timings. It is worth pointing out that this IC has very high tCCD (that is tRDRD and tWRWR) requirements. Some samples may need more than tCCD 4 at 1200 MHz, which is the auto value on most motherboards. tCCD (both RDRD and WRWR) also scales with voltage, meaning that the voltage requirements will be higher if somewhat reasonable tCCD is to be attained at 1400+ MHz. Thus, the practical usefulness of the low absolute voltage requirements for frequency is debatable, given that high tCCD is detrimental to performance.

4 Gbit P-die/V00H (C9BDZ, C9BGG, D9SGQ, D9SHB)

Used on Crucial and Micron modules from the late DDR3 era. Potentially also used on some modules from other brands with JEDEC specs. Likely best to avoid buying Crucial modules new, since you’re likely to get these ICs on them.

Maximum clock seems to be around 1100–1200 MHz. Timings are rather poor. Expect 14-14-10 at 1200 MHz for an average sample, or 12-12-9 at 1100 MHz for a better sample. Usually needs CWL 8 at these speeds but will run tRRD 4-16. tRFC is among the worst for 4 Gbit ICs, requiring around 240 at 1200 MHz. No timings scale notably with voltage.

Nanya

1 Gbit A-die

This is almost guaranteed to be the same die as Qimonda 1 Gbit. Look up the Inotera joint venture between Qimonda and Nanya for more info, which later turned into a joint venture between Micron and Nanya.

While they do not clock particularly high, capping out around 1000 MHz, they also don’t require much voltage for this frequency, unlike all other ICs of the time. Most are fine at their maximum frequency in the 1.2 V range. One may only speculate whether or not this has anything to do with Qimonda’s supposedly advanced and energy efficient technologies of the time. Timings are fairly poor, commonly 11-10-6-19 where no timings appear to scale at all with voltage. tRFC is also unimpressive at around 80 ns, or 80 ticks at 1000 MHz.

2E0C3CA696260EA285966AA7768EA3CF63C8B3CDAC15E796C46610209AE8E1A9

2 Gbit E-die

Only ever seen on a Corsair ver 8.14 kit, curiously of 1600 8-8-8 bin. These results are based on testing of those two sticks.

Maximum frequency is 1100 MHz and not much voltage is required for it, with requirements in the 1.2 V range. No amount of voltage could get 1200 MHz stable (was lucky to get it to POST) even with tCCD 6. Minimum timings were 11-11-8-30 for both samples with very minimal timing voltage scaling. On one sample, going from 1.2 to 2.1 V increased maximum CL 10 frequency from 1000 MHz to 1100 MHz, with half of that increase coming from just 1.2 to 1.4 V. tRCD showed even weaker scaling, with max tRCD 10 frequency only going from 1040 MHz at 1.3 V to 1090 MHz at 2.0 V. tRP scaling was similar, with max tRP 7 frequency going from 970 MHz at 1.2 V to 1015 MHz at 2.0 V.

tRFC and CWL do not scale meaningfully above 1.5 V. At 1100 MHz, minimum tRFC was around 125 ticks, or 114 ns. tWR may need to be higher than 5 depending on the sample.

2 Gbit G-die

For Nanya 2 Gbit B-die, see Micron D9LGK; they are almost certainly the same fundamental IC.

Nanya 2 Gbit G-die is fairly common, appearing on a large portion of Corsair's 4 GB standard bin Vengeance modules from 2011–2013. Also used on Nanya OEM modules from this time period, as well as some from Ramaxel.

Characteristics are similar to OEM D9PFJ. The clock limit is commonly 1066–1100 MHz, though some modules reach 1200 MHz while others get stuck at 933 MHz. Timings are typically 10-11-9-23–11-12-11-25 in the 1.5 V range at 1100 MHz if the sample can hit that speed. In general, modules from late 2012 and 2013 seem to be better than earlier modules, both for frequency and timings. tCAS scales relatively poorly; tightening it by 10% around 1.65 V requires on average a 17% voltage increase. tRCD and tRP only scale minimally. Expect around 105 ns tRFC.

2 Gbit F-die

Maximum frequency is around 1200 MHz. Raising tRDRD and/or tWRWR 5 helps bring down frequency voltage slightly, which may stabilize 1300 MHz, though this is almost certainly not a worthwhile trade-off for performance.

Timings are reminiscent of G-die. Expect 10-12-10-28 at 1200 MHz with around 1.65 V. tCAS scales ideally with voltage until 1.7 V or a bit higher, with lesser scaling at higher voltages. tRCD and tRP only scale minimally. For tRCD, going from 1.2 to 2.2 V dropped it enough for roughly a full tick decrease at fixed frequency or 100 MHz increase at fixed tick tRCD, with most of that scaling in the lower end of the range. tRP did not scale as clearly. On one sample, there was no apparent scaling for full stability above 1.6 V, while another sample scaled up to 2.07 V on tRP. With that said, the scaling was very minimal when present.

At 1200 MHz, tRFC runs at around 130 ticks or 108 ns, with a few ticks of voltage scaling, though mainly below 1.65 V. Expect CWL 7 1.65 V with higher voltage not impacting it much. Lower voltages may require 8. Depending on the sample, tWR higher than 5 may be required.

2 Gbit I-die

Similar to F- and G-die above. Maximum frequency is around 1200 MHz. Raising tCCD doesn't help much, at best only bringing down frequency voltage requirements somewhat and maybe stabilizing the next higher frequency step, which is likely not a worthwhile trade. Expect 11-12-9-26 timings at 1200 MHz with around 1.65 V, and tCAS dropping if voltage is pushed higher. tRCD, tRP, tRFC and CWL voltage scaling is similar to but slightly better than F-die above. tRFC and CWL also run very similar values as F-die above, with tWR once again potentially needing to be higher than 5 depending on the sample.

4 Gbit B-die

Given the early revision letter, one might expect these to only appear on early 4 Gbit modules, though they've been spotted on modules as late as the end of 2014. Rarely appear on Corsair modules with standard DDR3-1600 XMP of version 8.21, as well as Nanya OEM modules of the corresponding part numbers.

For single sided modules, maximum frequency is impressive, reaching 1500 MHz and above given enough voltage. 1400 MHz should be easily achievable with 1.7 V or less. Typical timings at around 1.65 V would be 11-13-11-28 at 1200 MHz or 13-15-13-31 at 1400 MHz. Double sided modules seem to not clock as high and often max out around 1200 MHz, with increased voltage not helping frequency much.

At below 1400 MHz, minimum voltage scales at 80–100 mV per 100 MHz. Maximum stable voltage also scales negatively with frequency, though even 2.0 V at 1500 MHz should be fine, so it is likely not a concern for practical applications. tCAS voltage scaling is a bit lower than ideal at low voltages, and starts to get quite bad at above 1.7 V. From 1.8 to 2.0 V, it is approximately

half of ideal scaling on average. tRCD scales reasonably well at very low voltages, with only slight scaling in the 1.6 V range and above. tRP conversely scales slightly negatively with voltage at all but very low voltages.

tRFC is insanely low for a 4 Gbit IC at around 120 ns depending on voltage, which matches some of the worse 2 Gbit ICs. With high voltages, it can even be pushed below 110 ns. CWL scales with voltage, needing 8 at 1.35 V but dropping to 6 at 1.80 V tested at 1200 MHz. 5 was not possible at up to 2.1 V.

4 Gbit Nanya B-die appears to be Micron design ID V70A, based on the 42 nm node. In other words, it is based on the same node as D9PCP (V70S), which in contrast is one of the worst 4 Gbit ICs. One might imagine that a lot changed in all those revisions from (V70)A to S.

The following article alludes to B-die being V70A:
https://iknow.stpi.narl.org.tw/Post/Read.aspx?PostID=11833

4 Gbit C-die

4 Gbit C-die is much like Micron V80B/J-die; timings are poor and frequency is poor for 4 Gbit. Avoid it if possible.

4 Gbit D-die

4 Gbit D-die is mostly seen in various Corsair ver 8.23 modules from the later DDR3 era. Appears in both standard DDR3-1600 modules as well as in some DDR3-2400 modules.

Maximum frequency is fairly variable. Some modules need increased voltage just to reach 1300 MHz, while others will go as high as 1466 MHz at around 1.8 V. Typical timings at 1200 MHz would be 11-13-12-30 at 1.5–1.7 V. Only tCAS and frequency scale significantly with voltage.

Elpida

1 Gbit BASE/BABG

Found on various early 1 and 2 GB modules with specs typically no better than DDR3-1600 8-8-8.

BASE may clock as high as 1000 MHz and slightly higher on some samples, while around 900 MHz is more typical for most. 7-8-5 or tRP 6 should be possible at these frequencies, with

voltage varying depending on the sample. tCAS, tRCD and tRP all scale with voltage, though tRCD and tRP scale less than tCAS.

BABG is basically just a slightly worse version of BASE.

1 Gbit BASE Hyper

These are a special version of BASE that are significantly better. Found on kits with XMPs such as 1600 6-6-6, 1866 7-8-7 and 2000+ 8-8-8/7-8-7. It's worth noting that these like to die, rarely while in use and usually in transport or storage, so they have become quite rare to find in working condition.

Maximum clock varies based on the sample, commonly maxing out around 1200 MHz for stability in SuperPi 32M. At 1000 MHz, 6-7-5 or tRP 6 should be achievable on most reasonable samples with enough voltage. While they are commonly binned for minimum voltage at this frequency and timing set, it is not a great indicator of the sample's benchmarking performance potential. Binning for maximum frequency at 6-7-5/6-7-6 at the maximum voltage they scale to (or what your preferred motherboard supports) is generally a better indicator. Some people also bin for the ability to run 1000 MHz 6-6-4, any voltage.

Like with normal BASE, all three primary timings scale with voltage, but tCAS scales the best. tRAS runs tighter than most Elpida ICs, with 20 or slightly lower being common at 1000 MHz. tRFC is also quite low for 1 Gbit ICs.

1 Gbit BBSE/BBBG

There seems to be no significant difference between the two versions on average, and they are hence commonly both referred to as BBSE, as it is significantly more common than BBBG. Found on 2 GB modules with fairly tight tRCD and often flat timings at XMP, such as 1600 7-7-7, 1866 8-8-8 and 2000+ 8-9-8/9-9-9.

Maximum frequency tends to be somewhere around 1300 MHz. This makes BBSE mostly suited to Ivy/Sandy Bridge and potentially older platforms, since these will not be limited by the IC's clock. Maximum stable voltage, largely unaffected by settings, is rather low. It is fairly variable, going as low as 1.75 V and as high as the 1.9 V range. There are seemingly also some "tricks" to get even higher voltages working, like running on low-load platforms such as X58, though the practical usefulness of such "tricks" is debatable.

Timings are fairly variable to start with, and the high variability in maximum voltage compounds this. tRCD falls between 7.62 and 8.44 ns (1066–1180 MHz tRCD 9) and is largely unaffected

by voltage. For tCAS and tRP, good samples would be expected to run 1100 MHz 6-x-6 (ideally tRCD 9), though most samples will hit the maximum stable voltage before the voltage required for this timing set. For higher frequencies, 1300–1333 MHz 8-11-7 CWL 6 is another relevant timing set to bin for. Really good samples should even do tRCD 10 at 1300 MHz.

Due to the low maximum voltage limits, absolute voltage requirements on BBSE are largely irrelevant. There are no practical differences between two modules that can run the same settings at their maximum stable voltages, even if this may be 150 mV higher for one of them. As such, avoid binning for “feel-good” settings like minimum voltage for 1100 MHz 7-10-7.

Characteristics also seem to vary a fair bit between platforms. For example, X58 may be able to run a timing set that is not possible on Z97. However, unless the plan is to use the modules on X58 or other older platforms, I would refrain from binning on them since it may give a false perception of the modules’ potential. Modules which are strong on Haswell have not been shown to have any issues on older platforms and it is thus a safe (but sometimes annoying) platform to bin on.

1 Gbit BDBG/BDSE

Found on various 2 GB modules with standard bins like 1600 9-9-9 from late 2009 and 2010. BDBG is also used on some fairly high bin modules, mainly from Kingston.

tCAS scales well with voltage across the entire stable voltage range, which is usually to well above 2 V. Significantly above 2 V may prove to be unstable regardless of settings, marking an absolute maximum voltage. tRCD scales slightly with voltage at lower voltages (<1.5 V) before scaling negatively with higher voltages, above roughly 1.6 V. This negative scaling gets worse as the voltage is increased further. tRP scales ideally at lower voltages, usually up to around 1.75 V but to a large extent dependent on the sample, with lesser scaling at higher voltages. tRAS (effectively tRC) and tRFC also scale notably with voltage. One may find that tRAS and tRFC can run the same tick value at multiple frequencies, assuming voltage is minimized for a constant CL.

One notable aspect about these ICs is the way CL and CWL interact. Together, they constitute the tCAS voltage requirements. The CL/CWL progression is as follows, in increasing difficulty (in terms of voltage requirements and stability):
CL 10 CWL 7
CL 9 CWL 6 (though CWL 7 is often required to prevent random freezing)
CL 8 CWL 6 or CL 7 CWL 8
CL 7 CWL 6 or CL 6 CWL 7
CL 6 CWL 5
CL 5 CWL 5 (impossible at any reasonable frequencies)

The variation on these is quite large. BDSE has lower variation, consistently being worse than reasonably good samples of BDBG. BDBG on the other hand varies from being just as bad as bad BDSE at the bottom end, to as good as reasonable PSC samples on the high end.

For BDSE and worse BDBG, 1200 MHz 9-12-9-29 CWL 6–7 in the 1.7 V range or 10-12-10 CWL 7 at around 1.6 V is common. These samples would be expected to run CL 8 CWL 6 or CL 7 CWL 8 at around 2 V, but this usually requires tRCD to be increased to 13. Some samples will hit higher frequencies, but I would say this isn't the case for a majority of low bin or unbinned samples. Reasonably good BDBG samples can have the voltage requirements 200 mV or more lower, with very good BDBG approaching reasonable or even good PSC. For BDSE, the absolute best samples can do 1200 MHz 7-11-8 CWL 8 or CL 8 CWL 6 at 1.8 V, which is about what would be expected from reasonably good BDBG.

1 Gbit BFBG/BFSE

Only used on DDR3-1600 modules and lower to my knowledge, mostly from 2010. In fact, it seems to make up a majority of 2 GB 1333 and 1600 9-9-9 modules from this time period. Possibly also used in some tighter bins, though unconfirmed.

CL, CWL and frequency interact in odd ways. Many samples don't like above CL 10 at high frequency, which will limit the maximum clock at a given voltage (or at the maximum voltage it scales to). At 800 MHz, CWL 6 or 7 compared to 7 or 8 can often be traded for one tick of CL. This behavior does not seem to exist at 933 MHz and CL-CWL-freq interactions at 1066+ MHz are all over the place, sometimes exhibiting this behavior and other times very different behavior.

There is typically one CL jump that will not benefit the voltage requirement, though where it is exactly varies. It can be from CL 6 to 7, 7 to 8 or possibly even 8 to 9 at CWL 7. At CWL 6, this will often move up one tick. However, even if the CL jump does not benefit the voltage requirement at fixed CWL, it may benefit CWL at a fixed voltage. Also of note is that the IC seems to be picky about CL 5. In some testing, CL 5 only worked at a very specific CWL (auto, value not noted). In later testing, I was not able to get CL 5 to work with multiple different CWL values tested.

Even when discounting the effects of the non-beneficial CL jump, all 3 primary timings may or may not scale non-linearly with frequency. This is typically very minimal for tRCD and may simply be caused by the increased heat at higher frequencies. tRP often exhibits linear scaling with frequency, but sometimes needs to be raised significantly beyond what would be expected at 1000+ MHz to maintain full stability. However, in these cases tRP values as much as 3 lower than the one required for full stability will still POST, just not be fully stable.

A module might see the following scaling at the same voltage:
800 MHz 6-8-6 CWL 7
1066 MHz 10-11-11 or 10-11-8

Maximum voltage is typically between 1.77 V and a bit below 2.0 V, where higher voltages than this cause instability no matter the settings. This is somewhat similar to how BBSE behaves at high voltages. While tCAS and tRP appear to continue scaling past this maximum full stability voltage, it only helps for ability to POST, and not actual stability. In cases where frequency is likely limited directly by voltage and not CL interactions, the higher 1.8 V range seems to provide the best stability.

tRCD sometimes scales very slightly positively with voltage, typically doesn't scale at all or at least not enough to notice, and sometimes scales slightly negatively with voltage. tRCD is generally around 10 ns. Most modules will run 8 at 800 MHz, though slightly fewer run 11 at 1100 MHz or 12 at 1200 MHz. tRCD has not been able to go a full tick below 10 ns on any tested BFBG/BFSE samples, though it seems to not be too uncommon on the equivalent PSC die.

Really good samples would be expected to run 1200 MHz 8-12-7 CWL 7 in the 1.8 V range, while simply good samples will run 9-12-8 in the 1.7 V range. For slightly below average samples, 1066-1100 MHz 10-11-x at around 1.65 V is typical.

Since CL does not go below 6, 800 MHz performance is best characterized by CL 6 voltage, ability to run tRCD 8 and ability to run tRP = tCAS without increasing voltage. Good samples will run 6-8-6 CWL 7 at less than 1.5 V, while really bad samples might need close to 1.8 V for 6-9-7 or 6-9-8. However, due to the above-mentioned non-linear scaling and CL anomalies, good characteristics at low frequency may not necessarily correlate with good characteristics at higher frequencies.

2 Gbits

The most notable Elpida IC out of the various 2 and 4 Gbit ones is probably 2 Gbit BCSE/BCBG, given that it's used on something like 3/4 of all black Corsair Vengeance DDR3-1600 9-9-9 4 GB modules from the Sandy and Ivy Bridge era, and a lot of modules with similar specifications from other manufacturers. At best, you might run 1000 MHz with meh timings, but you'll generally be limited to 900–933 MHz with 10-10-9. tRFC of 100 or a bit higher is expected at 933 MHz. Frequency and all timings only scale very minimally with voltage.

2 Gbit BDBG is basically just BCSE but worse, often maxing out at 800-900 MHz and occasionally not even doing 800 MHz. Timings also seem slightly worse on average.

2 Gbit BASE is interesting for being the only 2/4 Gbit Elpida IC that isn't complete garbage. It is somewhat similar to 1 Gbit BASE/BABG, meaning it can do reasonable timings at lower frequency even if it doesn't clock especially high.

4 Gbits

4 Gbit BASE/BABG/EASE is likely the worst DDR3 IC that exists. It commonly maxes out at 666 MHz, and if it does reach 800 MHz, it is the only IC I have ever seen that needs the "standard" JEDEC CL of 11, with it not being unusual for it to need 11-10-9 timings. Nothing scales notably with voltage.

4 Gbit BBBG/EBBG is basically just a slightly stronger version of BASE/BABG/EASE. Tends to consistently do 800 MHz and will sometimes do 900 MHz. Expect timings like 10-9-8-16 at 800 MHz or occasionally CL 9, with tRFC in the 160 range. Nothing scales with voltage to a notable extent. I will note that I had some Kingston sticks with rebranded "B-die" ICs of some kind that behave like EFBG/BFBG. It is unclear if these are some for some reason unusually strong BBBG or if the labeling is just incorrect.

4 Gbit BFBG/EFBG is much like 2 Gbit BCSE/BCBG, only they seem to hit 1000 MHz a bit more frequently and that they need tRFC in the 160 range at 933 MHz.

PSC/Powerchip

1 Gbit

"PSC" without any specification generally refers to early 1 Gbit PSC, from 2009 and 2010. These are some of the most well-known ICs within the DDR3 overclocking community, due to their very tight timings and fairly high frequencies (usually enough to saturate average Haswell memory controllers). Present in most 2 GB modules with low rated tCAS and tRP, but higher tRCD, such as 1600 7-8-7, 2000 6-9-6 and 2400 9-11-9. Corsair ver 7.1.

Some samples (possibly PCB-related) won't reach 1300 MHz, but most should do 1333 MHz and above, at which point the memory controller is likely to be the limit anyways, since these ICs are very hard on memory controllers.

These feature many timing anomalies, and are often misunderstood. tCAS scales well with voltage to and beyond 2 V. tRP also scales well at lower voltages, but scaling gets weaker at higher voltages. On the other hand, tRCD scales negatively with voltage, starting as low as 1.6 V. This has led many people to think that PSC only scales with voltage up to anywhere between 1.75 and 2 V, when they were in fact hitting tRCD limits.

CWL also interacts in odd ways with CL. At 1200+ MHz, CL 8 CWL 6 is usually equivalent to CL 7 CWL 8 in voltage requirement. Similar behavior but not identical behavior is present at other CAS latencies and frequencies. If minimum CWL is not tested for, it may appear as if certain CAS latencies do not impact the voltage requirement. See 1 Gbit BDBG for more details.

Strong samples should be able to run 1300 MHz 8-11-8 CWL 6. Minimize voltage with looser tRCD first, and then test minimum tRCD (see negative scaling above). Since higher voltage requirements for tCAS/tRP can be compensated for with higher voltage, assuming tRCD is strong enough, exact voltage requirements are less important, though for those curious, less than 1.80 V would be good for 1300 MHz 8-x-8 CWL 6. Ability to run tRCD 10 at the minimum voltage for 1200 MHz 7-x-7 CWL 8 is also a good test that is somewhat easier to pass than 1300 MHz 8-11-8 CWL 6.

For “good enough” samples, being able to run 1333 MHz 8-12-8 CWL 6 is a good test. Once again, minimize voltage with looser tRCD, then test for tRCD 12 at the minimum voltage. Really strong samples would be expected to reach 1400 MHz 8-12-8 CWL 6.

tRFC is reasonably good for 1 Gbit ICs, though it does depend a bit on sample quality and voltage. At lower voltages, expect around 80 tRFC at 1200 MHz, but this may drop to around 70 at higher voltages. Samples that are strong in other characteristics are typically also a few ticks stronger on tRFC. If testing higher frequencies, it is further worth testing the tRDRD timing, as some samples will require 5 (instead of 4), or need extra voltage for tRDRD 4.

As a general rule, it appears that later first generation PSC is significantly worse on average, more comparable to Elpida BDBG (see above). People often speak of “X-series”, “T-series” and similar, where the letter is referring to the first character of the batch code, with earlier batches having the letter X.

Second generation 1 Gbit PSC is comparable to Elpida BFBG (see above), but appears to be somewhat stronger for tRCD on average and possibly slightly stronger on tCAS and tRP. It is mostly found on 1600 9-9-9 bins and some x-8-x, $x \in \{6, 7, 8\}$.

2 and 4 Gbits

PSC’s 2 and 4 Gbit options are generally like a slightly better version of the corresponding Elpida ICs. Luckily, they're quite rare so you shouldn't be that likely to encounter them.

Best ICs and recommendations

Top ICs

1 Gbit

1 Gbit BASE Hyper, BBSE and “PSC” are generally considered to be the go-to high performance DDR3 ICs. Hypers are known for doing tight primary timings and scaling well with voltage for all three primaries, typically at frequencies between 900 and 1100 MHz. Most reasonable samples would be expected to run 6-7-6 or 6-7-5 timings at 1000 MHz with reasonably low tRAS and tRFC, given enough voltage. This makes them the ideal choice for architectures that cannot handle higher memory frequencies, such as 775, Bloomfield and Sandy Bridge.

BBSE is often a good in-between alternative for frequencies of 1100-1300 MHz. tCAS and tRP both scale well with voltage, while tRCD exhibits no scaling. Maximum voltage is typically between 1.7-2.0 V, where higher voltages tend to cause instability regardless of timings. Good samples would be expected to run 1100 MHz 6-9-6 at the maximum voltage they scale to.

“PSC” (typically referring to early 1 Gbit dies made by PSC) is the ideal choice for high performance on later DDR3 platforms, mainly Haswell and X79, but also Ivy Bridge desktop. Reasonable samples would be expected to run 1333 MHz 8-12-8 CWL 6, usually at around 1.9 V. Strong samples can run 1300 MHz 8-11-8 CWL 6 or even 1400 MHz 8-12-8 CWL 6 for very strong samples. Frequencies higher than 1333–1400 MHz are typically not possible due to memory controller limits.

While the three previously mentioned ICs can run exceptionally tight timings, they also put high load on the memory controller and therefore limit the system to operation at lower frequencies. Samsung 1 Gbit G-die—a newer and moderately obscure (though at this point well-known in many communities) IC—is typically lighter to run, therefore allowing higher frequencies, while also being able to maintain reasonably low primary timings. It is similar to 2 Gbit Samsung D-die (which incidentally is made on the same node), but can run slightly lower tRFC due to being a 1 Gbit IC. One of the main advantages of G-die is that it can usually be found for reasonably cheap on Samsung OEM modules (which typically perform well), though reasonable PSC kits can often also be found for acceptable prices due to low demand for 2 GB modules.

Other notable mentions include Micron 1 Gbit D9GTx, which for better samples will run 1000 MHz 7-6-6 or 7-7-6 with enough voltage, usually beyond 2 V. Good samples of D9JNM are somewhat similar, usually maxing out at 7-7-7 timings with around 2 V and not scaling much with higher voltage. Elpida BDSE/BDBG also deserves a mention, as it is effectively budget PSC. In fact, due to a partnership between Elpida and PSC, they are likely based on the same architecture, though PSC typically performs better on average.

2 Gbit

Samsung 2 Gbit D-die is perhaps the most relevant high performance alternative for most users, as it is available in 4 GB modules, allowing 16 GB total system memory on typical desktop platforms. While it is generally untouched in timings at both low and high frequencies, very good bins of 2 Gbit Micron M-die can compete with it at frequencies of 1200 MHz and below. For example, a good Crucial bin of M-die might run 1200 MHz 9-9-9 at typical daily voltages, while a good bin of D-die would run 9-11-10. With that said, D-die remains untouched for higher frequency platforms like Haswell, X79 and Ivy Bridge with good IMCs, where good bins can run 1400 MHz 10-12-12 at daily voltages.

Other notable mentions include 2 Gbit CFR, which on good PCBs can run high frequencies and reasonable timings; better bins of 2 Gbit BFR, which typically run 1200 MHz 9-12-10–10-12-11; and Samsung 2 Gbit Q-die, which for better bins is similar to bad D-die. Another very impressive IC is 2 Gbit GFR, which would likely match or even outperform 2 Gbit D-die if binned, though it is extremely rare, making binning unpractical. Good Crucial bins of D9KPT/K-die may also be similar to the M-die mentioned above.

4 Gbit

4 Gbit ICs are generally best to avoid unless 8 GB modules are required. They generally require much higher tRFC than 1 and 2 Gbit ICs, which by itself is not ideal, but adding to that, none of the 4 Gbit ICs scale significantly on all primaries to high voltages.

The only notable 4 Gbit IC in many people’s minds is 4 Gbit MFR, largely because it is able to run very high frequencies for DDR3. Primary timings are also among the better for 4 Gbit ICs, though it gets beaten by Samsung B and Q-die as well as good bins of Micron E-die.

4 Gbit Samsung B-die runs low (for 4 Gbit) timings at low voltages. Reasonable samples would be expected to run 1200 MHz 10-10-12 at around 1.5 V, while really good sticks can run 9-9-11. Frequencies of more than 1200 MHz are typically not achievable unless running at low voltages (1.5 V and lower) with good airflow. Q-die is generally very similar, though does not get as good at the high-end. Typical timings would be 10-12-11 or tRP 12 at around 1.5 V, with most modules not scaling to the voltages required for CL9.

The two main options for consistently running higher frequencies are 4 Gbit MFR and BFR. MFR runs better timings, with good bins being able to run 10-11-10 at 1200 MHz around 1.5 V, though good MFR bins can often be very hard to find and expensive. BFR can often be found in generic bins from the late DDR3 era and is therefore a cheap option for high frequency. Good

bins can run 10-12-13 or even tRP 12 at around 1.5 V at 1200 MHz. BFR should be able to run 1466 MHz and higher if on a reasonable PCB, though not all generic-bin BFR comes on good PCBs.

An honorable mention also goes out to Micron E-die/D9QBJ. I am reluctant to recommend buying this unless pre-binned, due to the insanely large variation between samples. Good samples can run 1200 MHz 9-9-10 at 1.65 V and less, and some will run up to 1400 MHz (though timings often scale poorly at such high frequencies). However, you may also get a sample which is very strong for timings, but doesn't even run 1100 MHz fully stable. As such, I would generally recommend Samsung B-die or even Q-die instead for platforms such as X79 and Ivy Bridge desktop, but for Sandy Bridge desktop and other platforms limited to lower frequencies, good bins of Micron E-die should be a good option.

Cost-effective recommendations

4 GB modules

For 4 GB modules, there are many highly cost-effective options. Most of the following suggestions will be OEM modules, as these are sure to give you a specific IC, while they also typically sell for less than third party modules due to average buyers assuming they are inferior.

Double sided 2 Gbit C and D-die are very good options, even compared to most higher end third party modules. They can typically run 1200 MHz, with higher often being possible. OEM D-die is often similar to or slightly worse than mid-bin third party D-die. C-die OEM modules are typically slightly worse for all three primary timings when compared to D-die.

These modules can be found under the part numbers M378B5273DH0-CH9 for D-die and M378B5273CH0-CH9 for C-die. The CH9 at the end indicates the DDR3-1333 JEDEC bin and can be replaced by CK0 for the DDR3-1600 JEDEC bin. There is typically no significant difference between these bins, and I would simply recommend getting whichever is cheaper.

Double sided Hynix 2 Gbit CFR modules are also a good alternative, if Samsung modules are not available or reasonably priced. As an added bonus, Hynix OEM modules are blue which may fit in better with most systems. The part numbers to look for are HMT351U6CFR8C-PB and HMT351U6CFR8C-H9. Most will be able to run 1400 MHz assuming the platform supports it, though some are limited to less.

Single sided 4 Gbit modules are also an option, though in this case you ideally want to run two per channel for the best performance. The typical part number format is HMT451U6**X**FR8C-PB, where X is replaced by M, A, B or D for MFR, AFR, BFR and DFR. The PB at the end can also be replaced by H9 for the JEDEC DDR3-1333 bins, though these are less common.

Crucial modules with better bins such as DDR3-1600 8-8-8 or DDR3-1866 are often a good option. Prices are typically reasonably low due to the lower rated speeds, but there is often good room for overclocking. I would recommend avoiding Crucial's standard DDR3-1600 9-9-9 modules, as these are typically no better than other third party modules based on Micron ICs.

Corsair, Kingston and G.skill modules with Hynix ICs as identified by the sticker (see module manufacturers above) are also a reasonable option.

8 GB modules

For cost-effective 8 GB modules, I would recommend looking for third party modules based on Hynix, as per the sticker on the module in the case of Corsair, Kingston and G.skill (see module manufacturers above). These can typically be found in cheap DDR3-1600 bins from the later DDR3 era which overclock well. For Corsair modules specifically, version numbers 4.21 and 4.29 are also good options, where 4.29 should be relatively common on standard DDR3-1600 bins from 2015+.

For OEM modules, my main recommendations are HMT41GU6AFR8C-PB, HMT41GU6MFR8C-PB and M378B1G73QH0-CK0 (alternatively -YK0), as other OEM modules don't consistently run 1200 MHz.

Better bin Crucial modules, such as DDR3-1600 8-8-8 or 1800+, are also a good option, especially for platforms that are limited to lower frequencies. While most will run 1200 MHz and higher, some will be limited to 1100 MHz, even if the modules are very strong for timings at these lower frequencies.

XMP guide

This guide is intended to give you an idea of what ICs to expect in various XMP bins. Note that XMPs such as DDR3-1600 9-9-9 are not included since nearly every IC will be able to run those settings. Keep in mind that ICs which are typically found in tighter XMPs at a given frequency may also be used in looser XMPs, though less commonly.

For Corsair, use the version number on the sticker if available. For third party manufacturers that only state date code and IC manufacturer (such as Kingston and G.skill), use that information in combination with the information below to make an educated guess.

Certain brands, such as Crucial (Micron), Klevv (Hynix) and Elixir (Nanya) almost exclusively use ICs from their parent company. Disregard the information below for these brands.

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DDR3-2800+

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
4 GB 10-12-12	Any	2 Gbit S D-die	Guaranteed
4/8 GB others	2013+	4 Gbit MFR	Nearly guaranteed
4 GB others	2012	2 Gbit CFR	Guaranteed

DDR3-2600/2666

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
8 GB any	2013+	4 Gbit MFR 4 Gbit D9QBJ (rare)	
4 GB 10-12-12	Any	2 Gbit S D-die	Guaranteed
4 GB others	2013+	4 Gbit MFR 4 Gbit D9QBJ (rare)	Very rarely D-die
4 GB others	2012	2 Gbit CFR	Very rarely D-die

DDR3-2400

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
4/8 GB 11-13-13	2013	4 Gbit AFR 4 Gbit MFR	Sometimes Nanya, especially on Corsair
4/8 GB 11-13-13	2014	4 Gbit BFR 4 Gbit AFR	AFR early 2014, BFR late
4/8 GB 11-13-13	2015+	4 Gbit BFR 4 Gbit DFR	
4/8 GB 11-13-14	2014+	4 Gbit BFR	
4/8 GB 11-14-13	2013+	4 Gbit AFR	

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8 GB 10-12-12	2013	4 Gbit S B-die	
8 GB 10-12-12	2014+	4 Gbit S Q-die	
4 GB 10-12-12	2014+	4 Gbit S Q-die “2 Gbit” S Q-die	
4 GB 11-13-13	2012	2 Gbit CFR	
4 GB 9-11-11	Any	2 Gbit S D-die	Guaranteed

DDR3-2133

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
8 GB 9-11-11 8 GB 11-11-11	2014+	4 Gbit S Q-die 4 Gbit D9QBJ	Q-die most common by far
8 GB 9-11-11 8 GB 11-11-11	2013	4 Gbit S B-die	
4 GB 9-11-11 4 GB 11-11-11	2014+	4 Gbit S Q-die 4 Gbit D9QBJ 2 Gbit S Q-die	Occasionally also 2 Gbit D-die
4 GB 9-11-11	2013	4 Gbit S B-die 2 Gbit S D-die	If D-die, typically mid bin
4 GB 9-11-11 4 GB 11-11-11	Later 2011–2012	2 Gbit CFR 2 Gbit S D-die	If D-die, typically mid bin
4 GB 9-x-x 1.50 V	Any	2 Gbit D-die	Guaranteed, typically mid bin
4/8 GB 10-12-12	2013+	4 Gbit AFR 4 Gbit BFR	

4 Gbit MFR may occasionally appear in x-11-11 modules from 2013 and later

DDR3-1866

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
8 GB 8-9-9 1.50 V	2014+	4 Gbit S Q-die	

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8 GB 8-9-9 1.50 V	2013	4 Gbit S B-die	
8 GB 9-10-9	2013–2015	4 Gbit D9QBJ 4 Gbit AFR	AFR mostly for 2013
4 GB 8-9-9 1.50 V	2014+	4 Gbit S Q-die 2 Gbit S D-die	If D-die, typically lower bin
4 GB 8-9-9 1.50 V	2013	4 Gbit S B-die 2 Gbit S D-die	If D-die, typically lower bin
4 GB 8-9-9 1.50 V	2012	2 Gbit S D-die	Typically lower bin
4/8 GB 9-10-11	2014+	4 Gbit BFR	
4 GB 9-10-9	2011–2013	2 Gbit BFR 2 Gbit CFR 2 Gbit N G-die	2014+ likely to be 4 Gbit ICs
4 GB 8-x-x*	2010–2011	2 Gbit BFR	*Where usually tRP = tRCD - 1

DDR3-1600

Module size/XMP	Manufacturing date	Typical die(s)	Additional notes
8 GB 7-8-8 1.50 V	2014+	4 Gbit S Q-die	
8 GB 7-8-8 1.50 V	2013	4 Gbit S B-die	
8 GB 8-8-8 1.50 V	2013–2015	4 Gbit D9QBJ	
4 GB 7-8-8 1.50 V	2014+	4 Gbit S Q-die “2 Gbit” S Q-die 2 Gbit S D-die	
4 GB 7-8-8 1.50 V	2013	4 Gbit S B-die 2 Gbit S D-die	
4 GB 7-8-8 1.50 V	2012	2 Gbit S D-die	
4 GB 7-8-x 1.65 V	2010–2012	2 Gbit BFR	
4 GB 8-8-8	2010-2011	2 Gbit BFR	
4 GB 8-8-8	2012+	2 Gbit CFR 2 Gbit S D-die	2014+ likely to be 4 Gbit ICs

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Additional information

This section contains some extra notes and information that may be useful for overclocking or for getting a further understanding of DDR3 DRAM and platforms.

DRAM voltage tolerance

DRAM ICs

No DDR3 ICs are known to have reliability issues (as in may suffer permanent damage) with 2.0 V or lower; however, there has generally been little long-term testing of 2 and 4 Gbit ICs at high voltages, so this is not to say that 2.0 V is definitively safe to use long-term on all DDR3 ICs. If you want to be very safe, stick to 1.65 V, or the maximum XMP voltage if you are using an IC that has had XMPs rated higher than that. Otherwise, see the below discussion and make your own judgement.

Extrapolating general manufacturer voltage tolerance characteristics may give us a better idea of what ICs can tolerate high voltages. Samsung ICs in general are not known to have any issues running 2.0 V and above, neither on DDR3 nor DDR4 (and as far as my knowledge goes, DDR2 or DDR5). Based on this, I would personally feel confident in running 2.0 V and higher on all Samsung DDR3 ICs. Do however note that some Samsung ICs scale negatively on either frequency or certain timings long before that point.

Micron ICs are also not known to have any issues with high voltage, though there has been relatively little testing of Micron ICs newer than 1 Gbit V58B (both for DDR3 and DDR4) at high voltages when compared to Samsung ICs. It is worth pointing out Micron kept the absolute maximum voltage rating listed in their datasheets the same (at 1.975 V) until V90B, so based on this information alone, one might assume voltage tolerance did not significantly drop until then. Do however note that datasheet values are not definitive, and that it’s still possible for ICs with the same datasheet absolute maximum voltage ratings to have vastly different voltage tolerance in practice. Personally, I would not feel all that concerned about running 2.0 V on 2 and 4 Gbit Micron ICs, but given that almost all of them besides the special Crucial/SpecTek variants scale only poorly or even negatively with voltage above 1.65–1.80 V, I would avoid running higher than this in practice for that reason alone.

Hynix DDR4 ICs are known to be somewhat sketchy with voltage for the ones from the first half of the DDR4 era. This overlaps with the late DDR3 era, which puts some doubt on voltage

tolerance of late Hynix DDR3 ICs. Adding to this concern is the fact that Hynix dropped the datasheet absolute maximum voltage rating from 1.975 V to 1.800 V going from 4 Gbit MFR to 4 Gbit AFR. Based on this, I would personally stick to running no more than 1.75–1.80 V on 4 Gbit AFR and later. For 2 Gbit CFR and earlier, I would not be concerned about running 2.0 V, while I'd consider it more sketchy for later 2 Gbit ICs.

For Nanya 2 and 4 Gbit ICs, none of them scale well above 1.8 V anyways so I would avoid running higher for that reason alone. 1 Gbit C-die can be presumed to be the same design as Micron V58B, so we would not expect 1.9–2.0 V to be unsafe there, if it is even stable that high.

Elpida and PSC 2 and 4 Gbit ICs barely scale at all with voltage so there is next to no reason to be running high voltage on them. All the 1 Gbit ICs are known to tolerate high voltage, and maximum stable voltage or negative timing scaling is a concern long before exceeding safe voltages is.

CPUs and memory controllers

LGA 775 and 1366 are known to be very tolerant to high memory voltage, despite X58 boards giving warnings about voltages above 1.65 V. For Sandy Bridge, the CPUs/IMCs are known to take damage from repeated usage above 2 V. Exactly how much lower one would need to go to avoid any damage is not precisely known, but I would stick to 1.8 V or lower to be safe. Ivy Bridge is known to be more tolerant than Sandy Bridge, but exactly where the limit is isn't known. 2.4 V is fine for at least shorter benchmarking sessions, but it's unclear if voltages this high could cause issues over long-term usage. Given the expected failure mode (gate oxide breakdown) for the type of damage potentially caused by high DRAM voltage at the IMC PHY, we would expect the gap between what quickly causes damage and what's safe for long-term usage to be relatively small, so it is very unlikely that 2.0 V or even 2.2 V would pose any risk for daily usage. Haswell has been used extensively at 2.4 V and higher for hundreds of hours by multiple people so it appears rather voltage tolerant. Short-term exposure to 2.9 V has also been reported without any damage.

AMD FX CPUs are generally known to be very voltage tolerant and have been believed to be more tolerant than the contemporary Intel CPUs. Whether or not this is actually the case isn't known since neither Ivy Bridge, Haswell nor FX have been reported to die or take damage from too high DRAM voltage, but we can regardless presume them to be fine with 2.0 V and very likely 2.5 V as well. **AMD Kaveri-based APUs are known to quickly take damage from 1.8 V.** Given the probable failure mechanism (gate oxide breakdown), it is not impossible that even 1.75 V would be fine to use long term, but I would personally stick to no more than 1.65 V for daily usage. AMD sold AMD/Radeon Memory-branded products marketed for Kaveri-based APUs with 1.65 V XMPs, so we can see this as official confirmation from AMD that 1.65 V is fine for these CPUs. APUs prior to Kaveri are said to be as voltage tolerant as FX CPUs.

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Whether or not this is true is unknown, but they at least don't suffer from the unusually low voltage tolerance of Kaveri-based APUs.

Platforms

The platform you are using may have a significant impact on your overclocking results, especially when trying to push higher memory frequencies. Keep in mind that your maximum frequency will always be limited by the weakest link in the chain, which could be the memory sticks, the platform, or the motherboard.

Bloomfield/Westemere (X58/LGA 1366)

On Bloomfield, the uncore clock cannot be set lower than 4x DRAM clock. This will usually limit DRAM clock to 900–1000 MHz, as the uncore clock will already be at 3.6–4.0 GHz by then. With low QPI/IMC/VTT/uncore voltage, the maximum DRAM clock is usually even lower. This limitation is not as severe on Westmere, where the uncore clock only needs to be 3x DRAM clock at the minimum. This can allow you to run higher memory frequencies on Westmere than Bloomfield. For both architectures, the maximum memory multiplier is 5x on locked CPUs. For example, at 200 MHz BCLK, this means that the maximum functioning memory strap is 1000 MHz or DDR3-2000.

Many motherboards will warn users of setting DRAM voltages above 1.65 V. However, it was later speculated that this recommendation is not inherently about the DRAM voltage itself, but about the difference between DRAM voltage and QPI/IMC/VTT/uncore voltage. The maximum difference between these two should not exceed 0.5 V, which with a stock QPI/IMC/VTT/uncore voltage yields a maximum DRAM voltage of 1.65 V, but with a QPI/IMC/VTT/uncore voltage of 1.40 V, this instead increases to 1.90 V. Many users have used such voltages for years without issues so it should not be a concern to run daily. Other users have theorized that no such relationship between DRAM voltage and QPI/IMC/VTT/uncore voltage exist, and that the CPUs are just naturally tolerant of well above 2.0 V no matter the other voltages, however, this has to my knowledge not been tested long-term so use with caution for daily. For just shorter benchmarking sessions, 2.5 V and likely higher is known to be fine.

Lynnfield (LGA 1156)

The Lynnfield memory controller is fairly strong, usually being limited by the maximum BCLK for locked CPUs, since the maximum memory multiplier for those is 5x. At 220 BCLK, this

would yield a maximum functional memory frequency of 1100 MHz or DDR3-2200. Unlocked CPUs, i.e. the i7 875K, should be able to go a bit higher still on memory frequency.

Sandy Bridge (LGA 1155)

Sandy Bridge is typically limited to 1066 MHz or a little more, with 4 rank per channel memory configurations often being unable to run 1066 MHz with full stability. Do note that the maximum supported memory strap on retail Sandy Bridge is 1066 MHz, so higher would require increased BCLK. I've found no significant improvements from tweaking memory controller voltages on Sandy Bridge, and they are typically best left around the auto voltage.

Ivy Bridge (LGA 1155)

Ivy Bridge maximum frequency varies quite a bit depending on the specific CPU sample and memory configuration. 1200 MHz is a common limit, but with a strong CPU and suitable memory ICs, 1400 MHz and above is not uncommon. Generally, higher factory bin CPUs tend to have stronger memory controllers. Most i7s are able to do 1200+ MHz, while many i5 3570Ks are limited to 1100 MHz, and locked i5s often max out at 933–1100 MHz.

Increasing IMC voltages beyond stock generally doesn't have much of an impact. It can help a bit if a frequency is on the edge. 1.20 V for $V_{cc\text{-}SA}$ and $V_{cc\text{-}IO}$ should not be a concern. Even higher voltages are most likely fine but this has not been tested as much for long-term use, and is unlikely to help much to begin with. Of the two voltages, it is mainly $V_{cc\text{-}IO}$ that benefits from being higher, and $V_{cc\text{-}SA}$ can in many cases run as low as 0.8 V.

Unlike some other CPUs, Ivy Bridge CPUs are largely unaffected by timings and it is rare that loose compared to tight timings make a difference to maximum stable frequency. They may however struggle with very high CL, so it could be worth trying CLs no higher than 11-12 when pushing for maximum frequency. They are also generally less affected by the "lightness" of ICs and amount of ranks installed per channel. Many CPUs can run 1200 MHz with 4 ranks per channel but will run higher even with 2 or only 1 rank per channel.

Ivy Bridge-E (X79/LGA 2011)

Ivy Bridge-E on X79 usually maxes out at 1200 MHz with the standard 100 MHz strap (also known as 1:1 BCLK:PCI-E). The 125 MHz strap typically allows for much higher frequencies, with 1400 MHz or a bit less being the typical limit for quad channel, and 1500 MHz being

possible on CPUs with good IMCs in single channel. V_{cc-SA} and V_{cc-IO} (also known as V_{TT}) will help when pushing higher frequencies, which is most noticeable with the 125 MHz strap.

Haswell (LGA 1150)

The Haswell memory controller is generally very strong, and typically has no problems running 1466+ MHz on a good motherboard with light memory configurations. However, it is impacted quite significantly by “hard” memory configurations and tight timings. With low IMC voltages, even 1200 MHz may not be stable if running 4 ranks per channel of a hard-to-run IC such as 1 Gbit PSC, BBSE or 2 Gbit CFR.

For most typical daily memory configurations, the V_{cc-SA} is the main or only one that will have an impact. This voltage is close to 0.8 V by default, so it is fine to set a relatively high offset. If running 4 ranks per channel, increasing V_{cc-SA} may be required just for 1200 MHz. For 2 ranks per channel, it depends a lot on the IC. For example, 2 Gbit CFR may start needing a positive offset at just 1300 MHz and could need +300 mV V_{cc-SA} at 1400 MHz, while a lighter IC like Samsung 2 Gbit D-die may be fine at the stock V_{cc-SA} voltage even at 1400 MHz. For 1200 MHz with daily ICs, I would recommend +150 mV V_{cc-SA} and +1 mV on both the V_{cc-IO} voltages (just to make sure the motherboard doesn’t set them to something stupid high when on auto). For above 1200 MHz, +300 mV V_{cc-SA} and +100 mV V_{cc-IO} is a good starting point, with V_{cc-SA} offsets of +400 or +500 mV being worth trying at 1400 MHz and above with 2 ranks per channel or more of Hynix ICs.

When pushing high frequency (mainly 1600 MHz and above) on 1 rank per channel 4 Gbit MFR and likely other high-clocking ICs, all voltages start playing a significant role. All three IMC voltages may have ideal voltages that vary from CPU to CPU, where higher or lower makes stability worse. For V_{cc-SA}, this is commonly between +100 and +500 mV. $V_{cc-IO(analog)}$ seems to prefer between +100 and +300 mV, with higher than +300 mV not improving stability in my testing and very often making it worse. While a positive offset is not always required, I have not noticed any benefit from running $V_{cc-IO(analog)}$ lower than +100 mV. $V_{cc-IO(digital)}$ often seems to like higher offsets of at least +200-300 mV. In my somewhat limited testing, I have not found a CPU that did not benefit from at least +100 mV.

For 1 Gbit PSC, I would describe the IMCs as not really scaling with voltage, but rather having specific minimum voltage requirements at certain settings. The reason I phrase it this way is because minimum voltage at a standardized set of timings and frequency says very little about how an IMC would handle a higher frequency with increased voltages. One sample might floor (+1/+1/+1 mV offsets) the IMC voltages at one frequency, but not be able to do even 10 MHz more with any IMC voltages. Another IMC might on the other hand require +1/+1/+100 mV at this same frequency, but be able to run significantly higher frequencies at higher IMC voltages.

Thus, I conclude that binning CPUs for minimum IMC voltages is not a viable methodology. Rather, IMCs should be binned for maximum frequency at sensible IMC voltages.

Regarding the voltages themselves, all three are relevant for stability, though behave differently. The SA voltage will often be fine with a +1 offset at the maximum frequency (up to +400 mV tested), but sometimes needs to be higher. More than a +300 mV SA voltage has not been required in my testing, though higher voltage has also not been observed to hurt stability. The IO(A) voltage fairly often needs to be +100 mV at the maximum stable frequency, and only sometimes needs to be even higher. The times when +100 mV was unstable, it was only slightly so and +150 mV would likely have been sufficient. On some samples, +300 mV IO(A) was observed to cause no-POST situations compared to +200 mV. For a few samples, even +100 mV yielded better stability than +200 mV. Finally, the IO(D) voltage is the main one that consistently needs to be set higher than +1 mV at the maximum frequency. This is also the only voltage that seems to sometimes exhibit some scaling (compared to just having minimum requirements), though this was not consistent across all tested samples. +300 mV is a reasonable starting point, and +350 mV or +400 mV can be tried if stability is on the edge at +300 mV. For some samples, this last 50–100 mV increase is the difference between getting a third or halfway into SuperPi 32M and consistently passing. The IO(D) voltage does not appear to experience significant negative scaling, though +350 mV was sometimes very slightly worse than +300 mV, with +400 mV sometimes showing more significant negative scaling. More commonly, increasing IO(D) simply does not affect stability outside of run-to-run variance.

For benchmarking with or binning 1 Gbit PSC (or strong samples of 1 Gbit BDBG), I recommend the following voltages:
+300-400 mV SA
+200 mV IO(A)
+300 mV IO(D) (with +350 or +400 mV being worth testing if on the edge)

It is likely that similar voltages would be suitable for other “hard” to run 1 Gbit ICs such as BBSE, though these are less likely to hit IMC limits due to not clocking as high.

DIMM PCBs

There exists a significant amount of baseless or misinformed speculation about DDR3 PCBs in online discussions, often presented as fact. I would be skeptical of any claims that aren’t backed up by either A/B testing or a large sample size.

There are a few different categories (largely based on manufacturer) of DDR3 PCBs: KO (Hsien Jinn), ST, Brainpower (BP), Levin (used on Crucial), “Kingston PCB”, “Samsung PCB” and “Hynix PCB”. Not many specifics are known about PCBs used on Micron, Nanya and Elpida OEM modules and these are therefore not covered.

Hsien Jinn offers a range of different PCBs:
KO-60247 – Single-sided 6-layer x8 UDIMM
KO-60244 – Double-sided 6-layer x8 UDIMM
KO-8114 – Single-sided 8-layer x8 UDIMM
KO-8117 – Double-sided 8-layer x8 UDIMM
KO-815x – Supposedly improved versions of KO-8117

Brainpower (BP) PCBs have markings starting with B63U (and ending in 0.70 or 0.71) for 6 layer PCBs and B83U for 8 layer PCBs.

ST offerings include the double-sided 8-layer ST-SG38U816 and double-sided 6-layer ST-G3U816.

“Kingston PCBs” are PCBs with markings starting with 2025, found on Kingston modules. These are speculated to all be 6-layer PCBs, since Kingston instead uses differently-branded 8-layer PCBs for high spec kits. 2025403 are double-sided x8 PCBs and 2025402 are single-sided x8.

There is no credible evidence for there being any significant differences in overclocking performance and ability between the various 8 layer KO, ST and Brainpower (B83U) PCBs. It is often claimed that KO-8117 or 8155 is better, but these claims are based on the fact that top bin G.Skill PSC and BBSE kits which naturally use the highest bin IC are most commonly shipped on these PCBs. This therefore makes it impossible to determine how much (if any) of the difference is from the PCB and how much is from the higher binned ICs, with it not being unlikely that all of the difference is from the higher binned ICs alone. To my knowledge, no A/B testing using the same set of ICs swapped between PCBs has been done with the different 8-layer PCBs.

In my own testing of IMCs on over 20 Haswell CPUs using 1 Gbit PSC-based DIMMs on both KO-8117 and ST 8 layer, I found differences in preference between CPUs. While most CPUs were able to reach higher memory clocks on the KO-8117 sticks, some reached higher clocks with the ST 8 layer sticks. This suggests that the two are at the minimum different in IMC load characteristics. While it may seem to suggest that KO-8117 is generally lighter on the IMC, it cannot be ruled out that this was due to the specific ICs on the KO-8117 sticks being easier to drive than the specific ICs on the ST 8 layer sticks.

In my testing of over 100 4 Gbit BFR-based sticks on various PCBs, I have consistently found sticks on 6 layer PCBs to experience a particular type of issues starting around 1333–1400 MHz. At these frequencies, instability with characteristics similar to IMC instability starts manifesting. Minimum voltage no longer scales with frequency in the expected manner at and beyond these frequencies, suggesting that the ICs themselves are not the cause of the instability. It is unclear whether it is the PCBs themselves or an interaction between the PCB and IMCs that are the limit, but instability has been largely similar between different Haswell CPUs, suggesting that it is

more likely to be the PCBs themselves rather than the PCBs influencing the IMCs (as we would expect different IMCs to have a notable impact in that case).

I have not encountered these types of issues on 4 Gbit BFR-based sticks on KO-8117 or Hynix OEM PCBs. When frequency is unstable on these sticks, the instability does not have characteristics of IMC instability, and minimum voltage also scales with frequency as expected to well above 1333–1400 MHz. The fact that Hynix OEM PCBs do not behave like KO/ST/BP 6-layer PCBs or Kingston PCBs and instead like KO-8117 would suggest that they may use 8 layers. Kingston PCBs behaving like 6-layer PCBs in this case is also further evidence for them likely being 6-layer.

In general, I have noticed similar issues with 2 Gbit CFR on 6-layer PCBs, where KO-8117 and Hynix OEM PCBs again do not have these issues. However, worth noting is that 2 Gbit CFR is seemingly rather hard on the IMC; for 4 GB Hynix OEM modules, SA voltage needs to be increased by quite a bit to consistently run above 1400 MHz. My limited sample size of 2 Gbit CFR on KO-8117 has not needed as much SA voltage for above 1400 MHz as the Hynix OEM modules, though the only 2 Gbit CFR modules I have tested on KO-8117 are G.Skill's top bins, so it is possible that the binned ICs may be lighter to drive for the IMC and that this is in fact not a result of the PCB itself. I have not noticed any PCB issues with 4 Gbit MFR, though it is worth noting that high bin 4 Gbit MFR gets shipped in kits with good PCBs, leaving only low bin MFR for use on kits with 6-layer PCBs. This means that it is still possible good MFR would encounter PCB limits if on 6 layer PCBs, just that no good MFR gets shipped on such PCBs to begin with.

Levin (Crucial) PCBs are presumed to be rather poor. D9QBJ on Micron OEM modules often seems to clock slightly higher than on Crucial modules with Levin PCBs. In addition, Crucial's special V80A variant typically does not go above 1200 MHz on the Levin PCBs, while the special SpekTek PEB12 variant used on Corsair modules has been seen reaching 1400 MHz and higher. With that said, those differences may be due to differences in characteristics between special Crucial V80A and special SpekTek PEB12 V80A, and not the PCBs themselves. Samsung OEM PCBs are generally regarded as poor, and I believe there are confirmed cases of overclocking characteristics improving after swapping ICs from Samsung PCBs to high-end PCBs. For ICs that don't consistently clock above 1300 MHz, I have either not noticed any differences between PCBs, or not noticed differences significant enough and with a large enough sample size to draw any definitive conclusions based on.

Identifying IC characteristics summary

tRFC tested at 1.65 V, 1200 MHz if possible, otherwise maximum frequency.

+ indicates that higher was not tested.

Hynix

IC	tRFC (ns)	Max CL	Max CWL	Typ. pkg. size
1 Gbit AFP	~60	11	8	8.0x11.0 mm
1 Gbit BFR	53–60	11	8	7.5x11.0 mm
1 Gbit TFR	65–70	13	9	7.5x11.0 mm
1 Gbit DFR	~70	15+	11	7.5x11.0 mm
2 Gbit AFR	~105	11	8	9.4x11.0 mm
2 Gbit BFR	83–91	15+	10	9.4x11.0 mm
2 Gbit CFR	73–83	15+	10	7.5x11.0 mm
2 Gbit DFR	~95	15+	12	7.5x11.0 mm
2 Gbit EFR	~115	15+	12	7.5x11.0 mm
2 Gbit FFR	~90	15+	12	7.5x11.0 mm
2 Gbit GFR	~100	15+	12	7.5x11.0 mm
4 Gbit MFR	179–200	15+	10	9.4x11.0 mm
4 Gbit AFR	156–169	15+	12	9.0x11.0 mm
4 Gbit BFR	168-180	15+	12	7.5x11.0 mm
4 Gbit DFR	~165	15+	12	7.5x11.0 mm

Samsung

IC	tRFC (ns)	Max CL	Max CWL	Typ. pkg. size
1 Gbit C-die	~62	11	8	
1 Gbit D-die				8.0x11.0 mm
1 Gbit E-die	~65	12	9	7.5x11.0 mm
1 Gbit F-die				7.5x11.0 mm

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1 Gbit G-die				~7.5x11.0 mm
2 Gbit B-die	~99	11	8	9.0x11.5 mm
2 Gbit C-die	90–100			7.5x11.0 mm
2 Gbit D-die	~80	14	10	7.5x11.0 mm
2 Gbit F-die	~118	15+	12	7.5x11.0 mm
“2” Gbit Q-die	~125	15+	12	~10.0x11.0 mm
2 Gbit S-die	~140	15+	10	~7.5x11.0 mm
4 Gbit B-die				10.0x11.0 mm
4 Gbit Q-die	192–205	15+	12	10.0x11.0 mm
4 Gbit D-die	~190	15+	10	7.5x11.0 mm
4 Gbit E-die	~160	15+	12	7.5x11.0 mm

Micron

IC	tRFC (ns)	Max CL	Max CWL	Typ. pkg. size
1 Gbit V48A	60–70	11	8	
1 Gbit V58B	~60	14	10	
2 Gbit V49A	~85	11	8	
2 Gbit V69A	~65	14	10	
2 Gbit V79B	105–115	14	10	
2 Gbit V79D	90–116	14	10	
2 Gbit V89C	100–120	15+	10	
4 Gbit V70S	~150			
4 Gbit V80A	150–175	15+	10	
4 Gbit V80B	~167	15+	10	
4 Gbit V90B	160–175	15+	12	

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4 Gbit V00H	~210	15+	10	

XMP and heat spreaders

It is often assumed that large or good-looking heat spreaders are beneficial (usually either in terms of lifespan or overclocking). This is often far from true. As already stated, the most important aspect for overclocking (and probably also lifespan, though memory tends to last too long to tell) is the ICs used on the individual modules. The heat spreaders have no impact on this, as manufacturers can put poorly performing ICs on modules with big/nice heat spreaders, or great ICs on modules without heat spreaders. The best example of this is perhaps Samsung's OEM modules based on 2 Gbit D-die, with (ugly) green PCBs and no heat spreaders. These will outperform something like 90–95% of third party modules with heat spreaders.

Some might argue that (big) heat spreaders should be beneficial, assuming that the ICs are good, as they would allow for better cooling and lower internal IC temperatures. While this is sound reasoning, it often falls apart in practice, due to poor heat spreader quality or crappy engineering. The biggest heat spreaders I've seen are those on OCZ's Reaper modules, with heat pipes and twice the height of most other RAM. On these, one of the sides of the module was not even in contact with the rest of the heat sink. Other heat spreader designs tend to use crappy double sided tape to connect the ICs to the heat spreaders, which many times doesn't make good contact, and even if it does, often acts more as insulation than a thermal transfer interface.

The XMP specifications tell you that the modules will run those settings. For standard DDR3-1600 XMP modules, this information is practically useless as almost all DDR3 ICs will run those settings. However, an XMP of DDR3-2933 tells you a bit more, as Hynix MFR is one of the few ICs that will run this speed. The same goes for XMP specifications like DDR3-2250 8-8-8 or 2000 6-9-6, as only one or very few ICs will run these settings.

In other words, don't assume that higher XMP speeds automatically imply better overclocking potential; many of Corsair's DDR3-2400 11-13-13 8 GB modules are based on 4 Gbit AFR, while some of their 1600 modules are based on the significantly better MFR IC.

Note that XMP stands for eXtreme Memory Profile; thus, saying "XMP profile" is equivalent to saying "extreme memory profile profile".

4 Gbit ICs, ranks per channel and performance

4 Gbit ICs will generally perform somewhat worse than 1 and 2 Gbit ICs at the same frequency and primary timings. This is because 4 Gbit ICs typically run worse secondary timings, both at auto and manually overclocked. This is most apparent for the tRFC timing, which usually runs at a minimum of 60-100 ns on 1- and 2 Gbit ICs, while 170+ ns tRFC is typically needed for 4 Gbit ICs.

Two ranks per channel (that is running either two single sided modules per channel or one double sided one) generally improves performance as well. This is because of multiple reasons. One reason is that more "rows" can be open at the same time, increasing the probability of "row hits", which improves performance. Another reason is that DDR3 RAM may be refreshed on a per-rank-basis (compared to bank-independent). What this means is that an entire memory rank will be refreshed at once. If there are multiple ranks, operations can still be performed on the other rank(s) that is/are not refreshing, leading to better performance. A third reason is that more ranks increase the total number of banks, which allows operations to be more parallelized.

Brief timing summary

First, some basic theory. DDR3 is organized in the following hierarchy:
(Channel) - Rank - Bank - Row - Column

For reading and writing operations, the row that is to be read from or written to must be open. This is accomplished by sending an ACTIVE command specifying which row in which bank is to be opened/activated. Next, a read or write command can be issued, specifying the bank and column that is to be written to or read from.

Note that different rows can be open at the same time in different banks and ranks; however, only one row can be open at a time in any specific bank. To operate on another row in the same bank, the current open one must first be closed by sending a PRECHARGE command to the bank in question. After the row has been closed by the PRECHARGE command, another one can be opened by another ACTIVE command.

DRAM needs to be periodically refreshed to retain the data stored in it. This is accomplished by issuing a Refresh command. Before a Refresh command can be issued, all banks must be precharged and idle.

(Note: some of the following info assumes AL = 0)

tCCD

tCCD specifies the minimum time between two consecutive column accesses (reads or writes). It is often replaced by timings such as tRDRD (Read to Read) and tWRWR (Write to Write). See the datasheet of your CPU for more details.

tCAS/CL

tCAS, also known as CL (CAS Latency) or tCL, specifies the time between when a Read command is registered by the DRAM and when the data is ready to be “extracted” from the DRAM. Note that the CAS latency is not the time between when the Read command issued and data is available, as signal propagation delays also play a role. Additionally, 2T command rate effectively increases CL by 1 (tick) compared to 1T, since commands are registered one clock cycle after they are first issued.

(t)CWL

CAS Write Latency, known as (t)CWL, (t)WCL or less correctly (t)WL, specifies the time between when a Write command is registered and when the first data can be "sent to" the DRAM.

tRRD/tFAW

tRRD specifies the minimum time between two consecutive ACT commands to different banks. tFAW specifies the duration of a window within which no more than 4 ACT commands may be issued. As this is generally not a limitation in practice, tFAW should be set to 4 * tRRD for best performance.

tRCD

tRCD specifies the minimum time between an ACT command and a column access (read/write) within the same bank.

tRP

tRP specifies the minimum time between a PRE command and any other command to the same bank.

tRAS/tRC

tRAS specifies the minimum time between an ACT and PRE command to the same bank. tRC specifies the minimum time between two ACT commands to the same bank. Typically, DDR3 SDRAM is limited by the time between two ACT commands, and not the time between an ACT and PRE command; however, since the minimum time between two ACT commands (tRC) will be limited by the minimum time between ACT and PRE (tRAS) plus the minimum time between PRE and any other command (tRP), the minimum effective tRC will be tRAS + tRP.

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Due to this redundancy, Intel processors have excluded the tRC timing and simply use tRAS (in combination with tRP) to control the effective tRC. As a result of this, you will be able to trade tRP for tRAS when tRAS is pushed to the limit. Since the tRP timing has a greater impact on performance than tRAS, make sure to tune tRP before tRAS to avoid such a scenario.

tRTP

tRTP specifies the minimum time between a READ and PRE command to the same bank. Since tRTP is typically lower than tCAS, this means that a row may be closed before the data read from it has "left" the DRAM.

tWR

tWR specifies the minimum time between the end of data input (end of a write burst) and a PRECHARGE command. Since read and write bursts last 4 clock cycles, and write bursts start CWL clock cycles after a WRITE command, the effective minimum time between a WRITE and PRE command is tWR + CWL + 4.

tWTR

tWTR specifies the minimum time between the end of data input (end of a write burst) and READ command. Similar to tWR above, this means that the minimum time between a WRITE and READ command is tWTR + CWL + 4.

tREFI

tREFI specifies the maximum average time between Refresh commands. For performance reasons, up to 8 Refresh commands may be postponed. Likewise, up to 8 Refresh commands may be "pulled in" (issued in advance), allowing for a longer period without the need for refreshing later. The maximum time between two consecutive Refresh commands may not exceed 9x tREFI.

tRFC

tRFC specifies the minimum time that must elapse between a Refresh command and any other command. As evident by this, refreshing "wastes" time that could be used for other operations; thus, lower tRFC and higher tREFI lead to better performance. The portion of time spent waiting for refreshing will be tRFC/tREFI.

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Formulas

Useful formulas for working with and overclocking DRAM.

Latency and timings

Latency based on timing and frequency:

Latency (ns) = timing (nCK) / frequency (GHz)

(Example: DDR3-2400 ≡ 1200 MHz = 1.2 GHz)

Timing based on latency and frequency:

Timing (nCK) = latency (ns) * frequency (GHz)

(Round up if unsure.)

Frequency and timing scaling

Expected timing at new frequency:

New timing = new frequency / old frequency * old timing

(Assumes perfect scaling. Must be applied to all timings. Round up if unsure. Useful for estimating timings at a different frequency, if timings at one frequency are known.)

Expected frequency at new timing:

New frequency = new timing / old timing * old frequency

(Assumes the limit is only the specific timing. Useful for estimating tRCD limits on BBSE/PSC)

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Micron die revisions, design IDs and nodes

1 Gbit die revision	Design ID (DID)	Manufacturing process
Rev. B (D9GTx)	V48A	78 nm [1]
Rev. D (D9JNx)	V48C	78 nm [1]
Rev. E	V58A	68 nm * [1]
Rev. F (D9KPT)	V58B	68 nm [2]
Rev. G (D9MNL)	V68A	50 nm [3], [4]
Rev. J	V88A	30 nm [3], [4]

2 Gbit die revision	Design ID (DID)	Manufacturing process
Rev. A (D9KLV)	V49A	78 nm [1]
Rev. B	V59A	68 nm * [1]
Rev. D (D9LGK)	V69A	50 nm [5]
Rev. H	V79B	42 nm [3], [6]
Rev. M (D9PFJ)	V79D	42 nm [7]
Rev. J	V89B	30 nm †
Rev. K (D9PSH)	V89C	30 nm [3], [5], [9]
Rev. N	V99B	25 nm * [10]

4 Gbit die revision	Design ID (DID)	Manufacturing process
Rev. A	V50A	68 nm * [1]
Rev. D (D9PCP)	V70S	42 nm [11]
Rev. E (D9QBJ)	V80A	30 nm [3], [12]
Rev. J	V80B	30 nm †
Rev. N (D9RVX)	V90B	25 nm [9]
Rev. P (D9SGQ)	V00H	20 nm [9]

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*Not known to have been mass-produced.

†Speculated/inferred

References for Micron die revisions, design IDs and nodes

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Hynix timeline

This is a rough timeline of the various Hynix ICs since late 2009. Note that ICs may be used in third party modules long after their EOL date, especially for more remarkable ICs such as MFR.

Die	First ES/sampling	Mass production	End of life
1 Gbit BFR	2009 Q2?*	2009 Q2?*	Late 2011/Early 2012
1 Gbit TFR	2009 Q3 (ES)	2009 Oct	Late 2011/Early 2012
1 Gbit DFR	2010 ~Aug (sampling)	2010 ~Nov	2013+
1 Gbit EFR	2012 June (ES)		2015+
2 Gbit BFR	Mid 2010 (sampling)	2010 Q3	2012 Aug
2 Gbit CFR		2011 Aug/Sep	2014 June
2 Gbit DFR		2012 June	2015 March
2 Gbit EFR	2012 Aug (sampling)	2012 Dec	2015 March
2 Gbit FFR		2013 Early	2020
2 Gbit GFR		Existed as MP in 2018	2020
4 Gbit MFR	2012 Apr (sampling)	2012 June	2013 June
4 Gbit AFR	2012 Aug (ES)	2012/2013 NY	2020+
4 Gbit BFR	2013 Dec (sampling)	2014 Nov	2020+
4 Gbit CFR	2015 Mar (sampling)	2015 Oct	2020+
4 Gbit DFR	2015 Apr (ES)	2015 Oct	2020+
4 Gbit EFR	2016 Aug (ES)		2020+

Source: Hynix product catalog through Web Archive

*The following press release claims TFR as second gen, and the BFR datasheet is dated 2010; however, there are BFR samples circulating from as early as 0920.
https://news.skhynix.com/hynix-introduces-the-second-generation-1gb-ddr3/

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Changelog

Version 4.00

Additions:

- 2 Gbit Samsung F-die
- 1 Gbit Samsung C-die
- 1 Gbit Samsung D-die
- 2 Gbit Nanya E-die
- 2 Gbit Nanya F-die
- 2 Gbit Nanya I-die
- Brief individual info for 2 Gbit BASE, BCSE/BCBG, BDBG, 4 Gbit BASE/BABG/EASE, BBBG/EBBG and BFBG/EFBG
- DRAM voltage tolerance section
- PCBs section
- Significantly more detailed Haswell platform info
- More detailed platform info for other platforms as well
- More IC decoding info for G.Skill and Crucial
- Info for a few more ICs in the identifying IC characteristics table

Changes/updates:

- Overclocking procedure section largely rewritten
- 2 Gbit Samsung D-die completely rewritten with more detailed info
- 4 Gbit MFR completely rewritten with more detailed info
- 4 Gbit DFR almost entirely rewritten with more info
- 2 Gbit EFR updated to include more info on frequency and tCCD
- V79D rewritten
- Minor updates to 1 Gbit Micron ICs
- Fixed some mistakes/typos in the Corsair version number table
- Various minor changes, mainly to IC characteristics reports

Version 3.1.0

Additions:

- 1 Gbit BBSE actual info
- Hynix 2 Gbit FFR
- Samsung 2 Gbit S-die
- Nanya/Qimonda 1 Gbit A-die

- More Corsair version numbers for Micron
- 2 Gbit Samsung C-die temperature data

Changes/updates:

- 4 Gbit Micron V80A completely rewritten (again)
- Some data in the Identifying IC characteristics table updated
- 1 Gbit BDBG/BDSE expanded
- Nanya 2 Gbit updated to include F- and D-die
- Some tREFI data removed since it depends much more on exact temperature than IC
- Various minor changes

Version 3.0.0

Additions:

- 17 different 1 Gbit ICs:
  1 Gbit Hynix AFP, BFR, TFR and DFR
  1 Gbit Samsung E-die, F-die and G-die
  1 Gbit Micron V48A, V48C, V58B and V68A
  1 Gbit Elpida BASE/BABG, BBSE/BBBG, BDSE/BDBG and BFSE/BFBG
  1 Gbit PSC (first and second gen)
- 2 Gbit Micron A-die/V49A
- 2 Gbit Samsung B-die
- 2 Gbit Hynix GFR
- 4 Gbit Nanya B-die
- Identifying IC characteristics table (tRFC, max CL/CWL, package dimensions)
- Bloomfield, Westmere and Lynnfield in Platforms
- Short explanation of test conditions for IC results, as well as a glossary

Changes/updates:

- 2 Gbit DFR rewritten from scratch with more detail
- 2 Gbit BFR tRCD and tRP voltage scaling clarified
- 2 Gbit CFR rewritten slightly
- 2 Gbit Micron D9PFJ slightly rewritten
- 4 Gbit Micron N and P-die no longer combined
- General subtiming section (“Going further”) slightly updated
- Some minor updates to IC recommendations
- Various minor changes

Version 2.3.1

Additions:

- Detailed tRCD and tRP voltage scaling info for many 4 Gbit ICs
- tRFC and tRRD info for most common 4 Gbit ICs
- Individual sections with more info for Nanya ICs

Changes/updates:

- Updates/clarifications to tCAS voltage scaling on some 4 Gbit ICs
- Micron 2 Gbit revision A design ID typo corrected
- Various minor changes

Planned additions:

- Common 1 Gbit ICs, likely with a focus on X58 and X79 use (for 12/16 GB total)

Version 2.3.0

Additions:

- Basic timing explanations
- 1 Gbit F-die in Micron die revision table
- Most common FBGA code for common Micron dies in Micron die revision table

Changes/updates:

- Slightly more info added to D9PFJ and D9PSH
- 2 Gbit CFR tRCD/tRP voltage scaling updated to be more detailed
- 2 Gbit DFR characteristics rewritten in a more logical way
- Nanya ICs are still called trash, but now in a few more words (might add even more in the future)
- The worthlessness of D9LGK is now elaborated on in a few more words
- Corsair Nanya version numbers updated to be a bit more detailed

Planned additions:

- tREFI for more ICs (mainly Samsung 4 Gbit, D9QBJ and possibly D9PFJ)

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Version 2.2.0

Additions:

- Micron die revision, design ID and manufacturing process table with sources

Changes/updates:

- Corsair version numbers updated

Planned additions:

- tREFI for more ICs (mainly Samsung 4 Gbit, D9QBJ and possibly D9PFJ)
- Basic explanations of common timings

Version 2.1.1

Changes/updates:

- Removed unintentional “sampling” note from 1 Gbit DFR in the Hynix timeline
- 1 Gbit TFR MP in Hynix timeline corrected from 2010 to 2009
- Nanya G-die updated to reflect very good samples

Planned additions:

- tREFI for more ICs (mainly Samsung 4 Gbit, D9QBJ and possibly D9PFJ)
- Micron design ID/revision table and possibly timeline
- Basic explanations of common timings

Version 2.1.0

Additions:

- tRAS info for most common ICs
- tREFI info for some common ICs
- Hynix/SK Hynix timeline since 2009

Changes/updates:

- Voltage/frequency scaling characteristics reformulated for 4 Gbit B and Q-die
- Notes added for late 2 Gbit EFR
- 4 Gbit DFR updated based on retest
- Various minor changes

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Planned additions:

- tREFI for more ICs
- Basic explanations of common timings

Version 2.0.0

Additions:

- Best ICs and buying recommendations
- XMP guide
- 4 Gbit Micron D-die (D9PCP)
- 4 Gbit Micron design ID V80B
- Ivy Bridge-E (X79) platform notes
- Useful formulas
- SK Hynix IC timeline (WIP)

Changes/updates:

- 4 Gbit Micron E-die (D9QBJ) revised
- Various minor changes

Planned additions:

- tREFI and tRAS characteristics for most common ICs
- Retest 4 Gbit DFR
- Finish Hynix IC timeline
- Basic explanations of common timings

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